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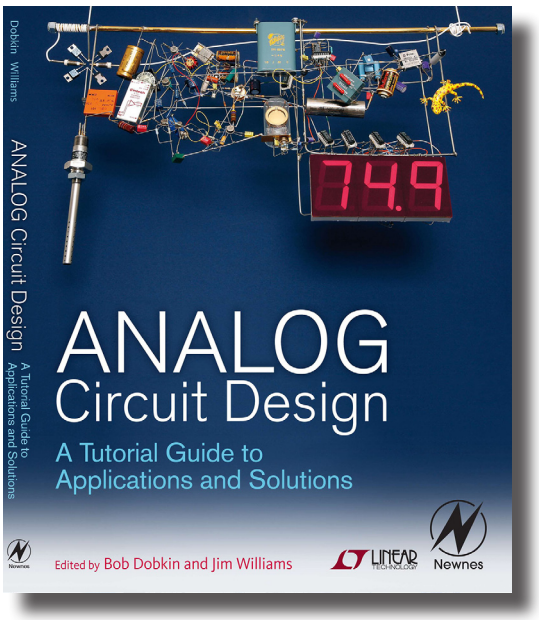
IN THIS ISSUE



Published September 2011 and now available. See page 2.

Fast, Accurate Step-Down DC/DC Controller Converts 24V Directly to 1.8V at 2MHz

Bud Abesingha

The continuous march in electronics toward lower supply voltages and higher load currents puts tremendous pressure on point-of-load DC/DC converters to maintain a fast pace of performance improvements. For instance, a lower supply voltage means a regulator must support a higher step-down ratio from a 12V or 24V power rail while maintaining high efficiency. Regulation accuracy also becomes more important as supply voltages drop—and accuracy must be maintained in the presence of parasitic IR drops and dynamic load transients. EMI generated by switching converters is also of concern, especially in RF applications.

Some applications require that their power supplies meet all of these stringent requirements: high power, high efficiency, high accuracy, high step-down ratio, fast transient performance and low EMI—and that they do it in a small footprint. The LTC®3833 is a high performance synchronous step-down DC/DC controller that steps up to the challenge. Figure 1 shows a typical application. The LTC3833 accepts an unregulated input voltage between 4.5V and 38V (40V abs max) and downconverts it to 0.67% accurate output voltage between 0.6V and 5.5V (6V abs max).

It features a 20ns minimum on-time, enabling a high step-down ratio (high V_{IN} to low V_{OUT}) at high frequency (up to 2MHz), and its control architecture is primed for fast transient performance. The LTC3833 is offered in 20-pin QFN (3mm × 4mm) and TSSOP packages with exposed pads for enhanced thermal performance.

(continued on page 4)

In this issue...

Linear in the News

ANALOG CIRCUIT DESIGN BOOK PUBLISHED

The much-anticipated book, *Analog Circuit Design: A Tutorial Guide to Applications and Solutions* was just published by Newnes, an imprint of Elsevier Science & Technology Books. Edited by industry gurus, Bob Dobkin and Jim Williams, the 960-page book covers a broad range of analog design topics. This is the first time that such an extensive collection of application notes has appeared in one volume from Linear Technology engineers.

Analog Circuit Design is a comprehensive source book of circuit design solutions that will aid systems designers with elegant and practical design techniques that focus on common circuit design challenges.

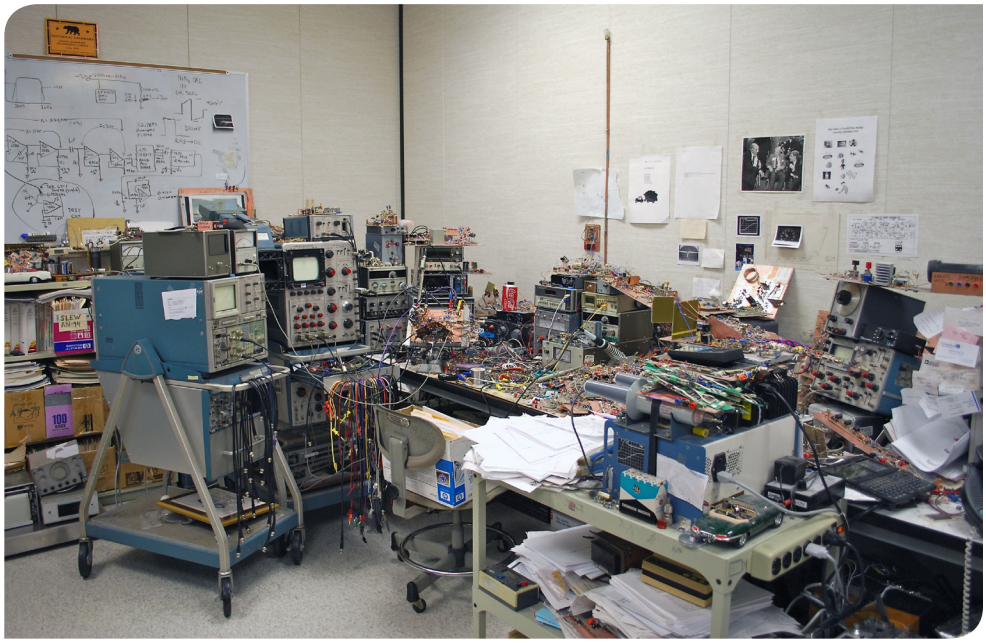
The book includes an extensive power management section, covering such topics as switching regulator design, linear regulator design, high voltage and high current applications, powering lasers and illumination devices, and automotive and industrial power design. Other sections of the book span a broad range of analog design areas, including data conversion, signal conditioning and high frequency/RF design.

Jim Williams wrote in the book's Introduction, "The nature of analog circuit design is so diverse, the devices so sophisticated, and user requirements so demanding that designers require (or at least welcome) assistance. Ultimately, the use of analog ICs is tied to the user's ability to solve the problems confronting them. Anything that enhances this ability, in both specific and general cases, obviously benefits all concerned."

Bob Dobkin stated in the book's Foreword, "One of the best avenues for learning analog design is to use the application notes and information from companies who supply analog integrated circuits. These application notes include circuitry, test results, and the basic reasoning for some of the choices made in the design of these analog circuits. They provide a good starting point for new designs.

"Since the applications are aimed at solving problems, the application notes, combined with the capability to simulate circuits on Spice, provide a key learning pathway for engineers. The analog information in most of these application notes is timeless and will be as valid twenty years from now as it is today. It's my hope that anyone reading this book is helped through the science and art of good analog design."

For more information, go to www.linear.com/designtools/acd_book.php. To purchase *Analog Circuit Design,* click on the Elsevier link for a 30 percent discount on the cover price, or go to the Amazon link at the bottom of the page.



Jim Williams' workbench

COMPUTER HISTORY MUSEUM EXHIBIT ON ANALOG & JIM WILLIAMS OPENS

The Computer History Museum in Mountain View, California has announced a new exhibit opening this month, "An Analog Life: Remembering Jim Williams." The exhibit, which runs from October 15, 2011 until April 15, 2012, will focus on how engineers work.

In their project overview for the exhibit, the museum's curator stated, "It is said that we spend about one-third of our lives at work. How we work is often reflected in the way we organize our desks and workspaces. Analog circuit guru Jim Williams' workbench tells us some things about the way he worked. For example, with its years-old strata of past circuits embedded in a matrix of thousands of overlapping components and still more circuits, we see someone who worked iteratively, drawing on past designs to continually invent new circuits and systems.

"Jim Williams' workbench is an inspirational object that allows Computer History Museum visitors to explore engineering work styles, be inspired by an extraordinary person and discover the world of analog circuitry and its impact on today's technology."

The centerpiece of the exhibit is Jim Williams' engineering workbench, which the museum carefully transported from his Linear Technology lab to the museum. The display will include interpretive graphics, explaining various aspects of analog design. In addition, the exhibit includes video interviews with engineers who worked closely with Jim Williams over the years, plus video footage of his labs, both at Linear Technology and at his home lab.

The "Analog Life" exhibit will launch on October 15, with an evening event at the Computer History Museum. Visitors to the launch will have an opportunity to view the exhibit, hear a panel discussion of analog experts discussing analog design and Jim Williams' contributions, and attend a book signing of the new *Analog Circuit Design* book with co-editor Bob Dobkin. For more information about the exhibit, visit computerhistory.org/highlights/analoglife.

A video interview with Linear Technology co-founders Bob Swanson and Bob Dobkin and CEO Lothar Maier can be found at www.linear.com/30yearinterview.

30 YEARS OF ANALOG INNOVATION

On September 26, Linear Technology commemorated three decades of innovation in analog integrated circuits. When the company was founded in September 1981, at the dawn of the digital revolution, some questioned the wisdom of founding a company focused purely on analog technology. Since then, the analog market has grown 20-fold with Linear contributing solutions to all corners of the electronics industry. The dawn of digital only *increased* the demand for analog.

Linear is consistently at the leading edge of new electronic markets as they have emerged. These include the PC revolution, laptop and tablet computers, industrial control and robotics, network infrastructure, cellular and satellite communications, automotive electronics including advanced displays, electronic braking and steering and now the growth of the hybrid/electric automotive segment, to name just a few. ■

The LTC3833 is a high performance synchronous step-down DC/DC controller that regulates to 0.67% output accuracy, operates up to 2MHz switching frequency and has a 20ns minimum on-time.

(LTC3833, continued from page 1)

FAST TRANSIENT PERFORMANCE AND CONSTANT FREQUENCY

The LTC3833 uses a new, sophisticated *controlled*-on-time architecture—a variant of the *constant* on-time control architecture with the distinction that the on-time is controlled so that the switching frequency remains constant over steady state conditions under line and load. This architecture takes advantage of all the benefits of a constant on-time controller, namely fast transient response and small on-times for high step-down ratios, while imitating the behaviors of a constant frequency controller.

The LTC3833 can respond to a load step immediately without waiting until the next switching cycle as in a conventional constant frequency controller. During a load step, the LTC3833 increases its switching frequency to respond faster and reduce the droop on the output. Similarly, during a load release, the LTC3833 reduces the switching frequency in order to prevent the input rail from charging the output capacitor any further. Once the transient condition subsides, the LTC3833 brings the switching frequency back to the nominal programmed value, or to the external clock frequency if it is being synchronized.

EFFICIENCY ↘		FREQUENCY, INDUCTANCE			
		200kHz, 2.00µH	500kHz, 0.82µH	1MHz, 0.47µH	2MHz, 0.20µH
V_{IN}	6V	91%	92%	91%	87%
	12V	92%	92%	89%	84%
	15V	92%	91%	87%	81%
	24V	91%	88%	83%	73%

Table 1: Example of efficiency variation over input and frequency. Higher frequencies have lower efficiencies but allow smaller component size for compact solutions. V_{OUT} = 1.8V I_{LOAD} = 10A.

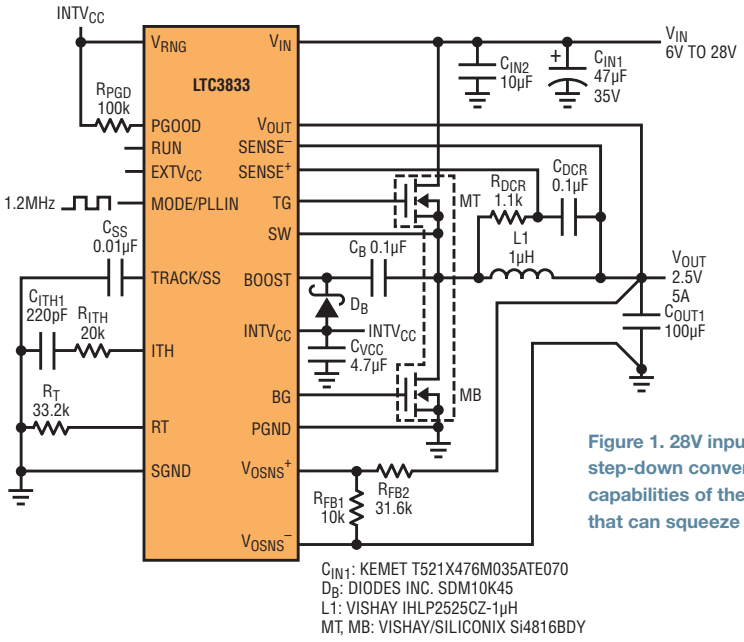


Figure 1. 28V input, 2.5V output, 5A, 1.2MHz step-down converter. The high frequency capabilities of the LTC3833 enable designs that can squeeze into tight spaces.

C_{IN1}: KEMET T521X476M035ATE070
D_B: DIODES INC. SDM10K45
L1: VISHAY IHLP2525CZ-1µH
MT, MB: VISHAY/SILICONIX Si4816BDY

The LTC3833's low minimum off-time of 90ns allows it to achieve high duty cycle operation and thus avoid output dropout when V_{IN} is only slightly above the required V_{OUT}. The low minimum off-time also factors into fast transient performance. If the switching converter's control loop is designed for high bandwidth and high speed, the minimum off-time of the LTC3833 does not limit performance. That is, in a load step condition, the time between consecutive on-time pulses can be as low as 90ns for a high bandwidth design.

Figure 2 shows a low voltage, high current application typical of a microprocessor power supply where the LTC3833 responds quickly to a 20A load step and release.

WIDE FREQUENCY RANGE FOR A MULTITUDE OF APPLICATIONS

The LTC3833 is capable of a full decade of switching frequency, from 200kHz to 2MHz (programmed with an external resistor on the RT pin). This wide range allows the LTC3833 to meet the requirements of a wide variety of applications, from low frequency applications that require high efficiency, to higher frequency

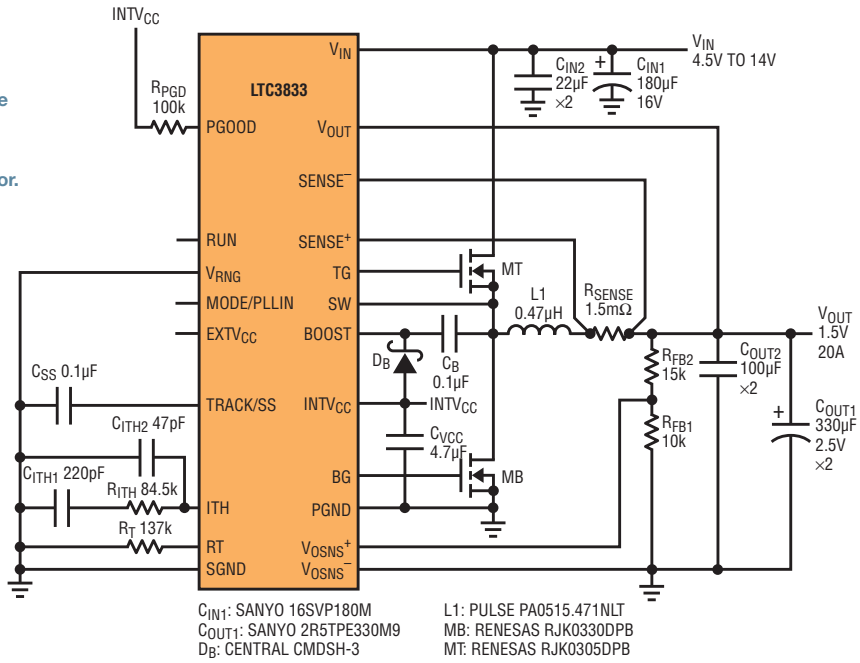


Figure 2a. 14V input, 1.5V output, 20A, 300kHz step-down converter. The LTC3833 excels in low voltage, high current applications such as these, which are typical of a microprocessor power supply. It can respond quickly to sudden, high slew current requirements of the microprocessor.

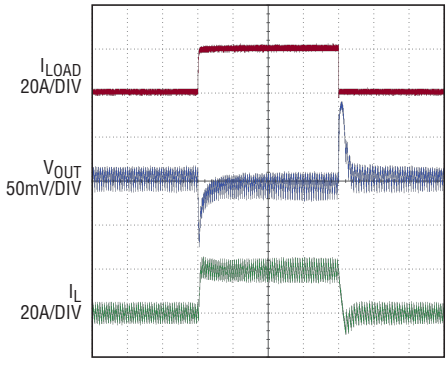
applications that require smaller solution size, to 2MHz applications that stay above the AM radio band while being able to downconvert from a high input rail and deliver high output current.

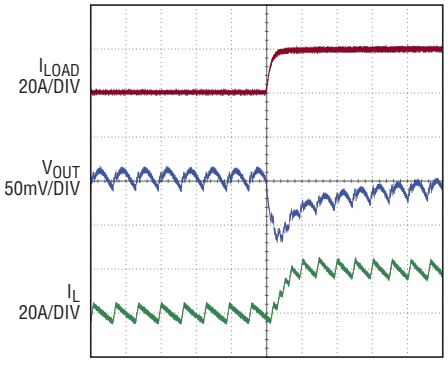
The choice of operating frequency is a tradeoff between efficiency and component size. Lower frequencies are more efficient due to a reduction of switching-related losses in the converter. On the other hand, lower frequencies require larger inductors and capacitors to achieve a given output ripple. At higher frequencies, smaller components can be used to achieve the same output ripple, but at the cost of efficiency. Table 1 illustrates the trade-offs between efficiency and inductor size required to maintain output ripple when the LTC3833 is used to generate a 1.8V output at several frequencies and input voltages. As seen from the table, switching losses are exacerbated at higher frequencies and higher V_{IN}, mainly due to the higher V_{DS} across the high side MOSFET.

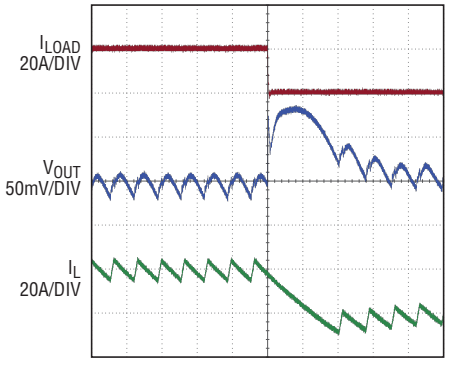
The LTC3833's wide frequency range also helps minimize EMI interference from the switching regulator. The switching frequency can be chosen, and held over line and load, such that the operating frequency and harmonics of the regulator fall outside of the frequency band of the end application. This allows the end application to easily filter out switching noise of the DC/DC converter. Figure 3 shows an example of a 5.5V application that operates above the AM radio band (f_{SW} > 1800kHz) that could be used to power electronics in an automotive infotainment system.

The LTC3833 provides an additional safeguard against EMI and noise interference by allowing it to be synchronized to an external clock applied to the MODE/PLLIN pin. This way, the end application has control over the DC/DC converter's switching cycles and timing so it does not interfere during critical time periods in the application where sensitive signal processing might occur.

Figure 2b. The LTC3833 can respond quickly to sudden, high slew current requirements.







High V_{IN}, high frequency applications are susceptible to minimum on-time limitations. Consider converting 28V down to 2.5V at 1.2MHz: this requires an on-time of about 74ns, which the LTC3833 easily achieves.

HIGH STEP-DOWN RATIOS AT HIGH FREQUENCY

The LTC3833 supports high side MOSFET on-times down to 20ns. This is important as lower minimum on-times translate to higher possible step-down ratios (V_{IN} to V_{OUT}) at a given switching frequency. Higher switching frequencies require lower on-times to achieve the same step-down ratio. Although the LTC3833's minimum on-time is a function of V_{IN}, V_{OUT} and switching frequency (see the data sheet at www.linear.com/3833 for details), it scales in the correct direction—the lowest minimum on-time is at high V_{IN} to low V_{OUT} at high frequency.

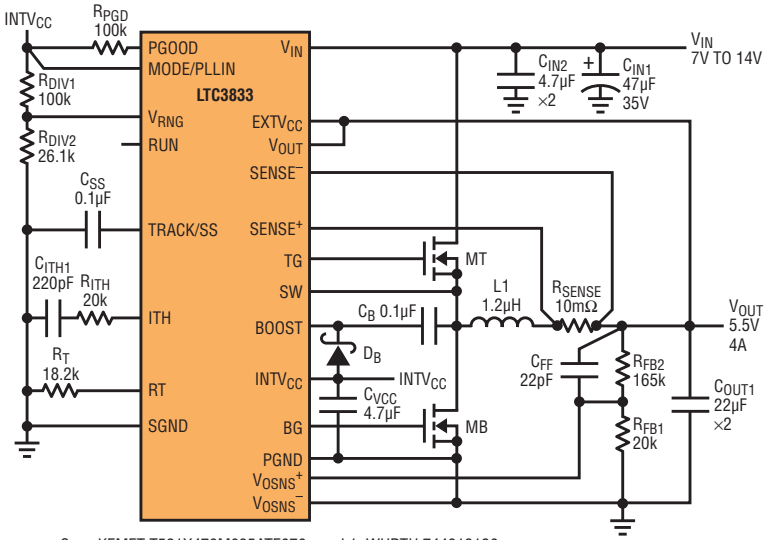
Of course, high V_{IN}, high frequency applications are susceptible to minimum on-time limitations. Consider the application in Figure 1 that requires converting 28V down to 2.5V at 1.2MHz. This requires an on-time of about 74ns, which the LTC3833 easily achieves. In contrast, most conventional current mode controllers cannot achieve 74ns of on-time. To run at high frequency, a conventional current mode controller would require two stages of DC/DC conversion, with stage one converting down to an intermediate voltage rail (e.g. 12V), and stage two converting to the final required voltage. This effectively doubles the solution size and degrades overall efficiency.

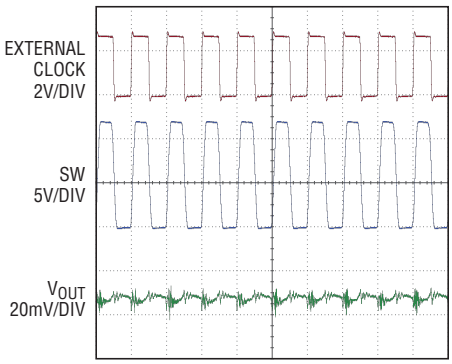
At very low on-times (20ns–60ns), the power MOSFETs' own switching delays can limit the minimum achievable on-time. Appropriate care must be given to choose power MOSFETs that have low turn-on and turn-off delays, and more importantly, little or no imbalance between their turn-on and turn-off delays. For example, most power MOSFETs' turn-off delay is about 30ns greater than their turn-on delay. This difference directly adds to the LTC3833's 20ns minimum on-time for an effective minimum on-time of about 50ns. Figure 4 shows a high step down ratio application operating at 2MHz where the high side power MOSFET has about a 12ns imbalance between turn-on and turn-off delays.

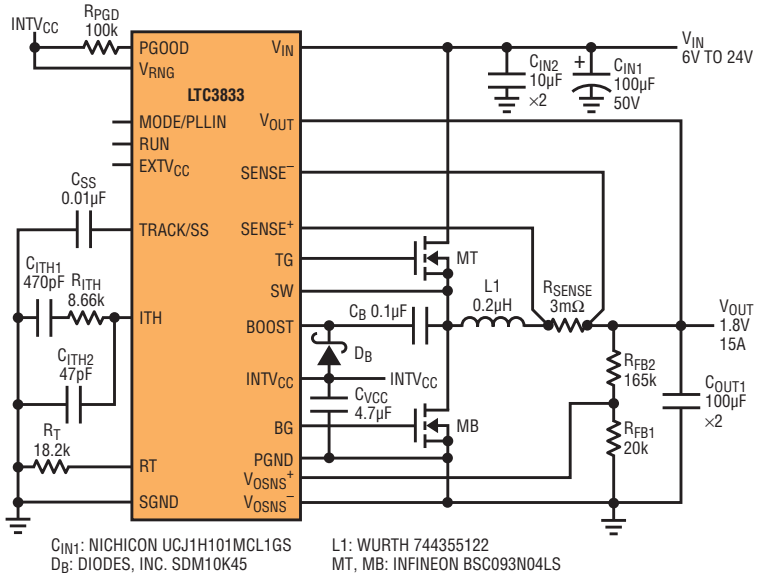
HIGH ACCURACY WITH MINIMAL EFFORT

The LTC3833 features true remote differential output sensing. This enables accurate regulation of the output even in high power distributed systems with heavy load currents and shared ground planes. Remote differential sensing is critical for low output voltages, where small offsets caused by parasitic IR drops in

Figure 3. 14V input, 5.5V output, 4A, 2MHz step-down converter. The LTC3833 can operate at switching frequencies above the AM radio band (f > 1.8MHz) allowing the AM radio to sufficiently filter switching noise and EMI emanating from the step-down converter.







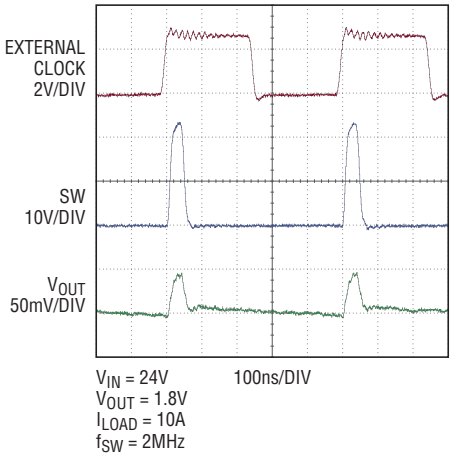


Figure 4. 24V input, 1.8V output, 15A, 2MHz step-down converter. The LTC3833 can achieve very low on-times, which allows for a single-stage converter design. Using a traditional controller with longer minimum on-times would require two or more stages, which would mean a costlier, bigger and less efficient design.

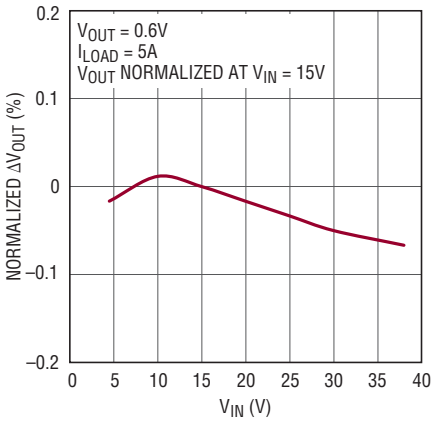
board traces can cost several percentage points in regulation accuracy.

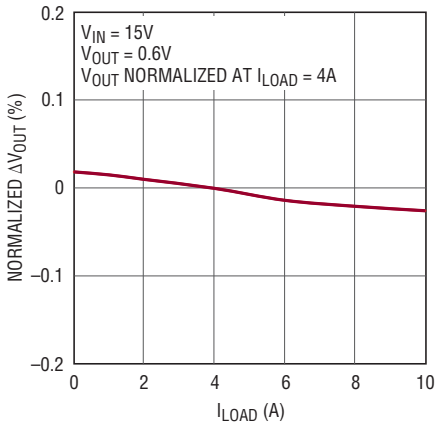
Remote differential output sensing and an accurate internal reference combine to give the LTC3833 excellent output regulation accuracy over line, load and temperature, even when there are offsets caused by trace losses on the PC board. The LTC3833 is able to achieve output accuracy figures of ±0.25% at 25°C, ±0.67% from 0°C to 85°C and ±1% from –40°C to 125°C. Total accuracy that accounts for line, load and remote ground variations are ±1% from 0°C to 85°C and ±1.5% from –40°C to 125°C. Figure 5 illustrates typical regulation accuracy that could be expected from the LTC3833 over line, load and temperature.

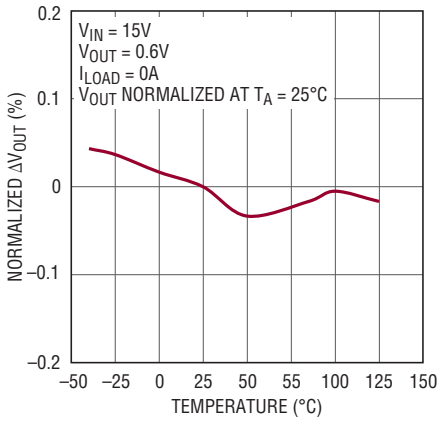
Conventional schemes for remote differential output sensing involves a unity gain differential amplifier that senses the remote output and remote ground terminals directly (Figure 6). The output of this amplifier is then scaled down through an external resistor divider (which also programs the output voltage) and fed back into the core controller. In addition to greater design effort involved with this scheme, input and/or output common mode range limitations of the unity gain amplifier can reduce the range of output voltages where remote differential sensing can be used.

Remote differential output sensing is seamless in the LTC3833. It is simple to use, requires minimal, if any, design effort, and requires less area than other remote sensing schemes. As in traditional feedback sensing, the output is sensed through a

Figure 5. Typical regulation accuracy of the LTC3833 over line, load and temperature







The LTC3833 features true remote differential output sensing. This allows for accurate regulation of the output even in high power distributed systems with heavy load currents and shared ground planes. Remote differential sensing is critical for low output voltages, where small offsets caused by parasitic IR drops in board traces can cost several percentage points in regulation accuracy.

resistor divider network that is used to program the output voltage. The LTC3833 takes this one step further by sensing the output's remote ground terminal where the other end of the resistor divider network is terminated. Therefore, output voltage programming is similar to other feedback-sensing controllers, but with the advantage that the LTC3833 is able to correct for board losses and offsets. The LTC3833 is invaluable when regulation accuracy is required in high power, high current distributed applications where multiple systems share power and ground planes.

The LTC3833 is designed to handle remote ground offsets as large as ±500mV with respect to local ground. This includes the ability to soft-start smoothly from an initial condition state where the output of the regulator is sitting 500mV below local ground.

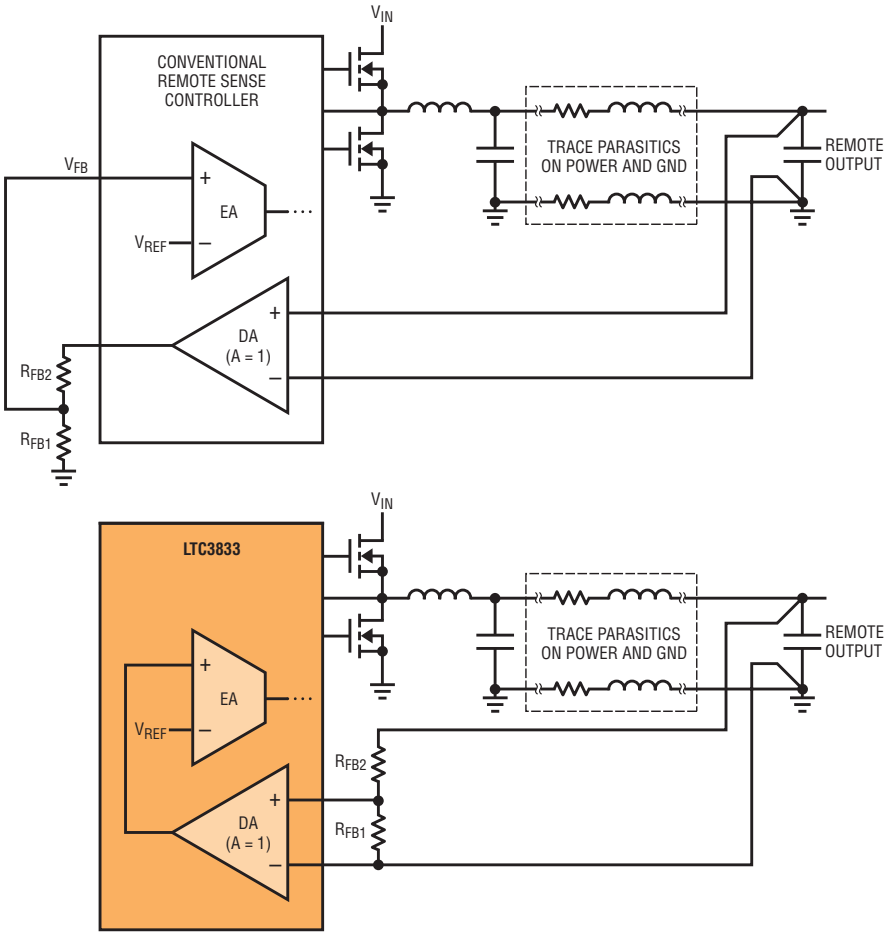


Figure 6. Conventional remote differential sensing involves more design effort and board space than remote sensing with the LTC3833.

OTHER FEATURES

Programmable Current Limit

As a valley current mode controller, the LTC3833 senses and controls the valley point of the inductor current in order to maintain output regulation. The inductor current is sensed with a sense resistor in series with the inductor or by sensing the inductor's DCR voltage drop through a RC network across the inductor. Either way, the inductor current is continuously sensed in all switching cycles, which allows accurate and fast control of the output current including output current limit.

The LTC3833 allows programming the output current limit through the voltage on VRNG pin, providing an extra degree of freedom when choosing inductors and sense resistors for a given application. The maximum current sense voltage across the sense resistor or inductor's DCR can be programmed continually from 30mV to 100mV. Figure 7 shows the maximum current sense voltage as a function of the VRNG voltage.

$EXTV_{CC}$ and $INTV_{CC}$

The LTC3833 has an internal 5.3V low dropout regulator that powers internal control circuitry including the strong high and low side gate drivers, and is available to the outside world through the $INTV_{CC}$ pin. The $INTV_{CC}$ regulator can source a maximum of 50mA while maintaining good regulation, so it can be used in moderation as a supply to power external circuitry or as a bias voltage source. An external supply source (≥4.8V) can be connected to $EXTV_{CC}$ pin to bypass the internal regulator. This is especially

The LTC3833 also features a continuously programmable current limit, $EXTV_{CC}$, selectable pulse-skipping or forced continuous modes, run enable, supply tracking and soft-start.

useful for high V_{IN} applications where the internal linear regulator becomes less efficient. If the LTC3833 switching regulator is generating a 5V output, it can be connected back to $EXTV_{CC}$ (shown in Figures 3 and 8). This scheme can increase overall efficiency by 2%–3% versus using the internal 5.3V regulator.

Pulse-Skipping or Forced Continuous Mode at Light Loads

The LTC3833 offers two modes of operation at light loads to best meet the requirements of a given application. For applications that require high efficiency at light loads, the LTC3833 can be programmed for pulse-skipping mode (by tying MODE/PLLIN pin to GND), which allows the switching regulator to transition into discontinuous conduction mode, thus increasing efficiency by lowering the number of switching cycles. The downsides of pulse-skipping mode are the variable switching frequency (dependent on load current) and a slightly higher output voltage ripple.

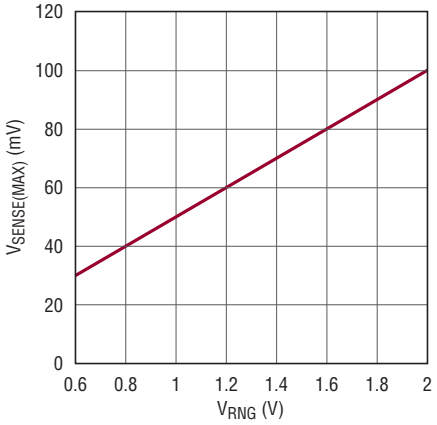


Figure 7. The LTC3833 provides a programmable current limit.

On the other hand, for applications that require predictable EMI performance and value constant switching frequency or require very accurate regulation at light loads, the LTC3833 can be programmed for forced continuous mode (by tying MODE/PLLIN pin to $INTV_{CC}$). In forced continuous mode, the LTC3833 maintains the programmed switching frequency even at no load, but sacrifices light load efficiency in the process. Figure 8 shows an example of the differences in efficiency between the two modes.

Soft-Start and Tracking

The LTC3833 provides soft-start—either from zero or prebiased output voltage condition (Figure 9)—and external tracking capability through the TRACK/SS pin. The soft-start time and ramp rate can be programmed by a capacitor from TRACK/SS pin to GND. This capacitance and the 1µA current source out of the TRACK/SS pin determine the soft-start time

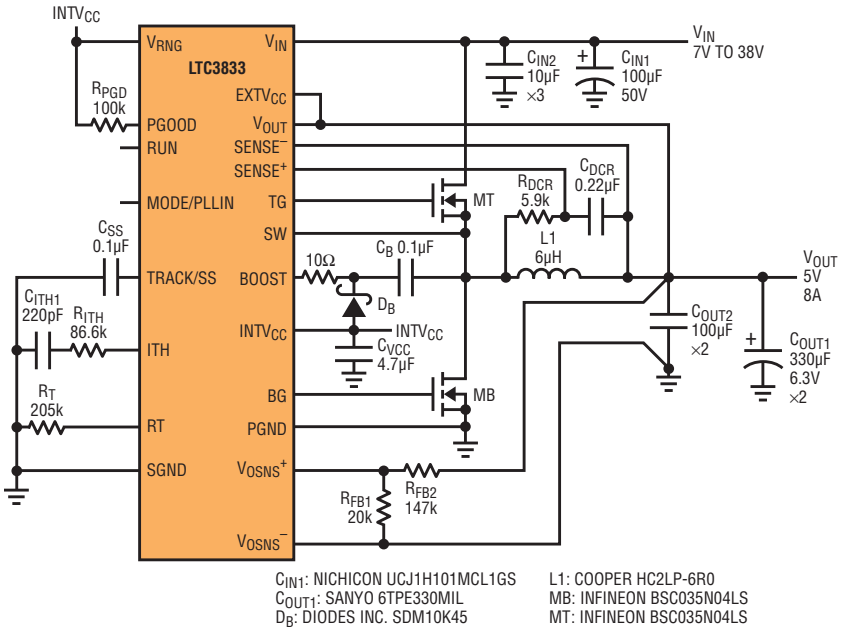
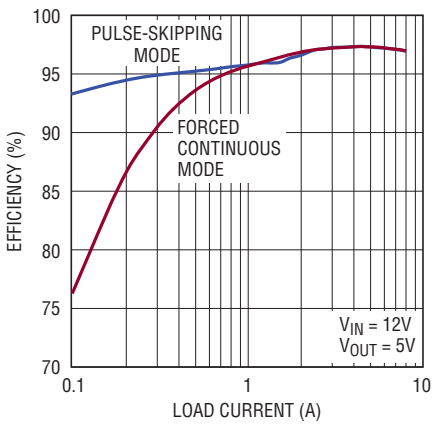


Figure 8. 38V input, 5V output, 8A, 200kHz step-down converter. The LTC3833 offers two modes of operation at light loads: pulse-skipping mode for higher efficiency or forced continuous mode for constant switching frequency.



The LTC3833 acts quickly and effectively to protect the output and external components of the switching regulator if the output encounters overvoltage, overcurrent and short-circuit conditions.

and ramp rate. The output reaches its final programmed value when TRACK/SS voltage reaches 0.6V, the internal reference voltage for the LTC3833. Alternatively, an external ramp can drive the TRACK/SS pin in order to track the output of the switching regulator to the external ramp, providing better control of power-up and power-down conditions of the switching regulator.

Run Enable

The LTC3833 provides a dedicated enable/disable function through the RUN pin. The LTC3833 self-enables when the RUN pin is left floating. It is disabled or shut down by forcing RUN to GND. The quiescent current of the LTC3833 in shutdown is 15µA. The LTC3833 is enabled when RUN is pulled greater than 1.2V, which is an accurate, well-controlled threshold. This allows the RUN pin to be programmed as an input undervoltage lockout if desired by programming a resistor divider from V_{IN} to RUN to GND. The RUN pin can also sink about 35µA of current, allowing it to be pulled directly up to V_{IN} through a sufficiently large pull-up resistor.

Power Good and Fault Protection

The LTC3833 acts quickly and effectively to protect the output and external components of the switching regulator if the output encounters overvoltage, overcurrent and short-circuit conditions.

The programmed current limit prevents overcurrent conditions and allows the output to droop down when the output current exceeds current limit. During short-circuit conditions, the LTC3833 forces foldback current limiting, where the current limit is progressively lowered to about a quarter of the programmed current limit for a hard short at the output (Figure 10).

Overvoltage conditions are handled by forcing the low side power MOSFET to turn on to discharge the overvoltage at the output.

The LTC3833 provides a power good function through the PGOOD pin, which is an open drain output that is resistively pulled up to a logic level voltage (or $INTV_{CC}$) externally. If the output is within ±7.5% of the programmed value, then PGOOD is high, indicating power is good.

CONCLUSION

The LTC3833 is a synchronous step-down DC/DC controller that can meet the demands of high current, low voltage applications while remaining versatile enough to fit a wide range of step-down DC/DC applications.

It provides the usual set of features such as soft-start, power good and fault protection commonly available with step-down controllers. It also adds some invaluable extras, including remote output sensing, programmable current limit, external clock synchronization and $EXTV_{CC}$. It also features high performance specs, including 0.67% output accuracy, switching frequency (up to 2MHz) above the AM radio band, high step-down ratios through a 20ns minimum on-time, and quick response time to transient conditions in the line and load. ■

Figure 9. The LTC3833 can smoothly start up into a prebiased output.

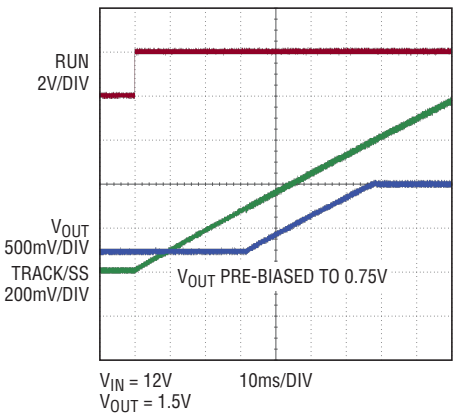
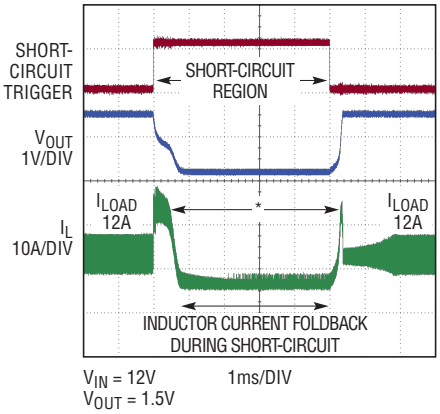


Figure 10. During a short circuit at the output, the LTC3833 reduces the output current to 1/4 of programmed current limit.



* INDUCTOR CURRENT REACHES CURRENT LIMIT BEFORE FOLDBACK AND DURING SHORT-CIRCUIT RECOVERY

2-Channel and 4-Channel Pin-Selectable I²C Multiplexer Features High Noise Margin, Capacitance Buffering, Level Translation and Stuck Bus Recovery

Rajesh Venugopal

The inherent simplicity of I²C and SMBus 2-wire protocols has made them a popular choice for communicating vital information in large systems. Both standards employ simple open-drain pull-down drivers with resistive or current source pull-ups. Nevertheless, several practical problems arise as systems grow in complexity.

The first problem with large systems is that devices with hard-wired I²C addresses require address expansion to prevent conflicts. Second, noise causes glitches that can be interpreted as legitimate clock or data transitions, compromising data reliability. Third, I²C devices can cause the bus to stick low. Finally, timing specifications are increasingly difficult to meet, and clock frequencies are limited by the equivalent bus capacitance, which increases with system size and complexity. The LTC4312 and LTC4314 pin-selectable 2-channel and 4-channel I²C multiplexers with bus buffers address these issues with a number of powerful features (see Table 1). Since these two devices share the same features, except for the number of channels, this article focuses on the LTC4314.

An upstream I²C bus (SDAIN, SCLIN) can be connected to any combination of downstream buses through the LTC4314's bus buffers and multiplexer switches by driving the ENABLE pins of the desired output buses high. Multiple devices having the same address can be placed on different buses and isolated using the ENABLE pins, thereby achieving address expansion.

The buffers provide capacitance isolation between the upstream bus and the downstream buses, allowing for partitioning of the bus capacitance. In single supply systems, the buffers regulate the bus up to 0.33 • V_{CC}, providing a large logic low noise margin. Rise time accelerators (RTAs) of appropriate strength can be activated to overcome bus capacitance limitations, reduce rise time and allow for higher switching frequencies even when operating with heavy loads.

The LTC4314 is compatible with the I²C standard and Fast Mode, SMBus and PMBus specifications. Stuck bus recovery circuitry disconnects the upstream bus from downstream buses when SDA and SCL have not been simultaneously high at least once in 45ms, freeing the upstream bus to resume communications. The recovery circuitry also attempts to convince

Table 1. Key features of the LTC4312 and LTC4314

FEATURE	BENEFITS
2- and 4-Pin Selectable Downstream Buses	• Maximum flexibility of bus configurations • Address expansion when used as a MUX
I²C Buffers	• Breaks up bus capacitance, which allows large I²C compliant systems to be built, by keeping the capacitance of each section < 400pF
Selectable V_{IL}	• High logic low noise margin up to 0.33 • V_{CC} • Selectable RTA Operating voltage range
Level Translation	• Provides I²C communication between 1.5V, 1.8V, 2.5V, 3.3V and 5V buses
Rise Time Accelerators (RTAs)	• Reduce rise time • Allow larger bus pull-up resistors for better noise margin • Selectable RTA pull-up current strength
Disconnection and Recovery from Stuck Bus	• Free masters to resume upstream communications • Generates up to to 16 clock pulses and a stop bit on the stuck buses to convince the stuck device to release high

The LTC4314 is compatible with the I²C standard and Fast Mode, SMBus and PMBus specifications. Stuck bus recovery circuitry disconnects the upstream bus from downstream buses when SDA and SCL have not been simultaneously high at least once in 45ms, freeing the upstream bus to resume communications.

the stuck device to release high by generating up to 16 clock pulses and a stop bit on the enabled downstream buses.

Finally, cards can be hot-swapped into and out of the LTC4314's I²C output buses provided that the channel being hot-swapped has been disabled. The LTC4314's operating voltage range is V_{CC} from 2.9V to 5.5V, V_{CC2} from 2.25V to 5.5V and bus voltages from 2.25V to 5.5V. The LTC4314 can level translate down to 1.5V and 1.8V buses under certain conditions if RTAs are disabled on the low voltage bus.

HIGH BANDWIDTH BUFFERS IMPROVE NOISE MARGIN AND SPEED WHILE MAINTAINING LOW OFFSET

High noise margin is obtained by leaving the LTC4314 buffers on until both the input and output bus voltages are > 0.33 • V_{MIN}, where V_{MIN} is the lower of the V_{CC} and V_{CC2} voltages. This is possible because the high bandwidth buffers do not limit the rise rate of the bus, permitting them to stay on to a higher bus voltage.

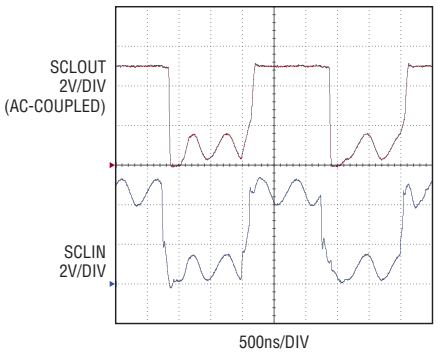


Figure 1. The LTC4314 transmitting a noisy 400kHz I²C signal applied to SCLIN. The SCLOUT1 waveform tracks SCLIN when SCLIN is a logic low. During logic highs, noise on SCLIN above 0.33 • V_{MIN} is not propagated to SCLOUT.

As seen in Figure 1, when a noisy 400kHz square wave signal is applied to SCLIN, the SCLOUT1 waveform tracks SCLIN when the SCLIN voltage is < 0.33 • V_{MIN}, and releases high when the SCLIN voltage is > 0.33 • V_{MIN}. The low offset makes the SCLOUT1 waveform almost identical to the SCLIN waveform for voltages < 0.33 • V_{MIN}. No output glitches occur as the input crosses the V_{IL} level of 0.33 • V_{MIN}, as seen in the SCLOUT1 waveform.

As the buffers are disconnected when both input and output bus voltage are > 0.33 • V_{MIN}, any noise applied to the logic high state on one side is not propagated to the other side as long as that bus voltage does not drop below 0.33 • V_{MIN}. This is seen in Figure 1 where the logic high state of SCLOUT1 is unaffected by noise on SCLIN.

Designers who are in control of the entire I²C system can set the LTC4314 to operate at frequencies of up to 1MHz by adjusting the RC load on the bus and using strong RTAs (see Table 2). The LTC4314's high-to-low propagation delay t_{PDHL} is always positive, on the order of 100ns. Depending on bus loading conditions on the upstream and downstream sides of the LTC4314, the low-to-high propagation delay t_{PDLH} of the LTC4314 can be either positive or negative. For systems operating at high frequencies (>400kHz) designers should quantify the t_{PDLH}-t_{PDHL} skew in their SDA and SCL pathways and ensure data set-up and hold times are acceptable on all buses.

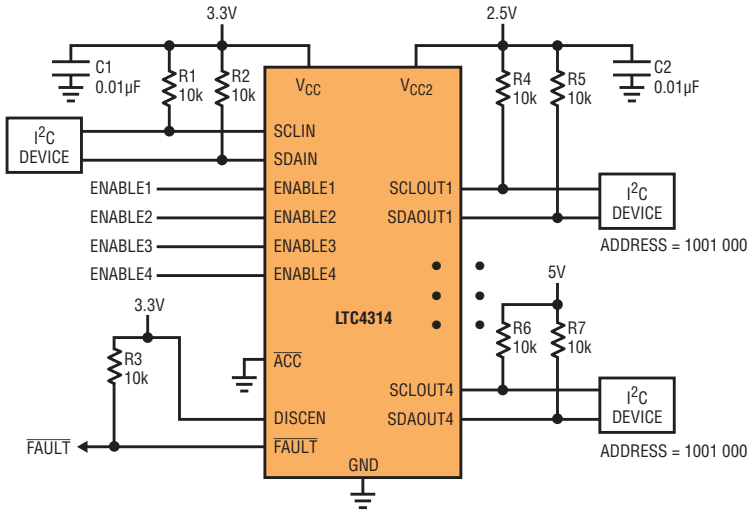


Figure 2. The LTC4314 in a nested addressing and level shifting application where a device on the upstream 3.3V bus communicates with devices on the 2.5V and 5V downstream buses. Only buses 1 and 4 are shown for simplicity.

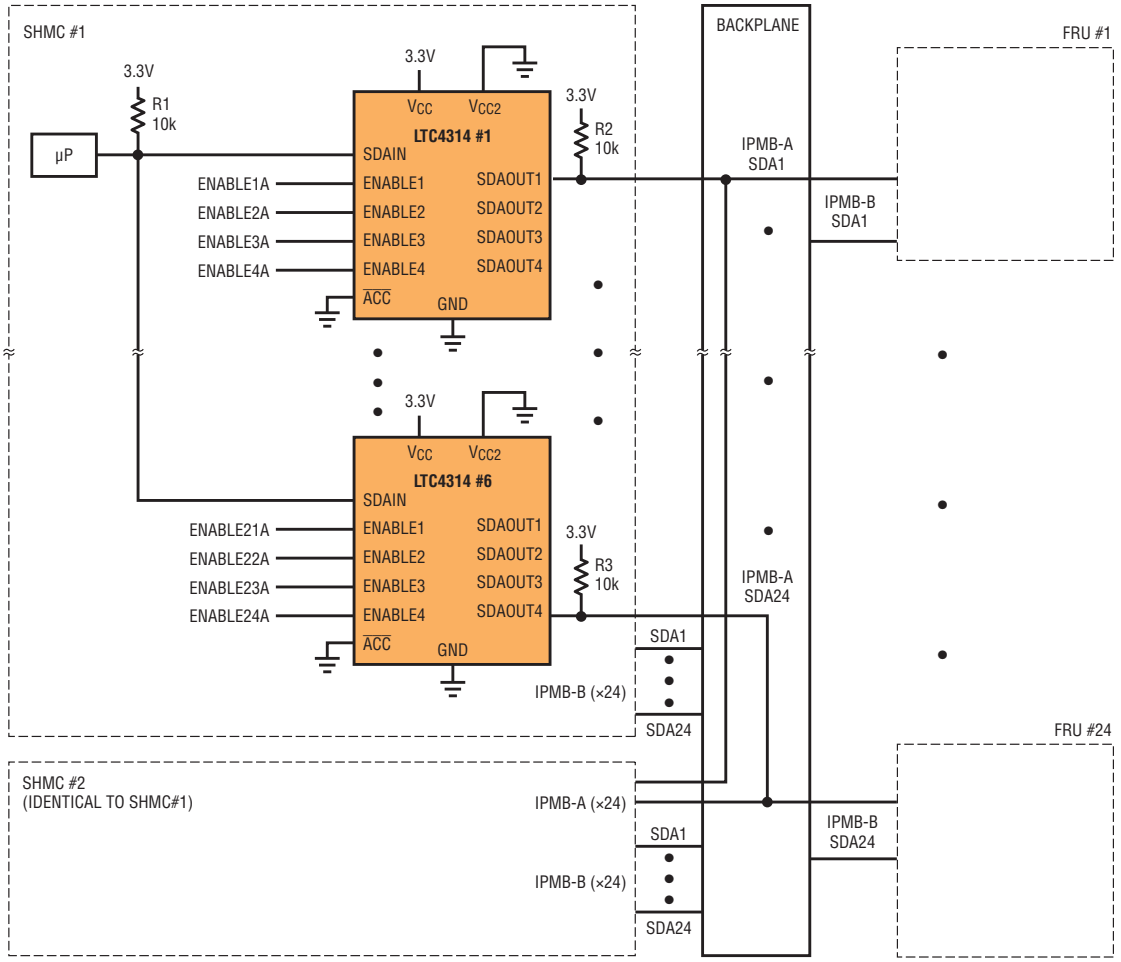


Figure 3. The LTC4314 used in a radially connected telecommunications system in a 6 × 4 arrangement. The ENABLE pins of only one shelf manager are high at any given time. Only the SDA pathway is shown for simplicity.

LEVEL TRANSLATION AND NESTED ADDRESSING

The circuit shown in Figure 2 illustrates level translation and nested addressing features of the LTC4314. The LTC4314 can level translate the input and output buses to voltages between 2.25V (1.5V and 1.8V under some circumstances) and 5.5V. In Figure 2 the LTC4314 translates a 3.3V input to 5V and 2.5V outputs. Only downstream buses 1 and 4 are shown for simplicity. Each output channel has a dedicated ENABLE pin select that allows the master to communicate independently with slave devices with identical I²C addresses provided that only one downstream bus is enabled at a time.

RADIALLY CONNECTED TELECOMMUNICATIONS APPLICATION

Figure 3 shows the LTC4314 used in a radially connected telecommunications application such as ATCA. Two shelf managers (SHMCs) are used to communicate with slave I²C devices for redundancy. Each shelf manager can have as many LTC4314s as required depending on the number of boards in the system and the desired radial/star configuration (6 × 4 in Figure 3). The ENABLE pins inside only one shelf manager are asserted high at any time. Since the LTC4314 can be cascaded with other Linear Technology bus buffers, up to 24 FRUs with Linear Technology bus buffers on their edges can be plugged into the backplane.

PARALLELING LTC4314s TO ACHIEVE MULTIPLEXING OF MORE BUSES

Multiple LTC4314s can be connected in parallel to perform higher order multiplexing. Figure 4 shows a 1:8 multiplexer using two LTC4314s.

INTEROPERABILITY WITH NONCOMPLIANT I²C DEVICES

The high buffer turn-off voltage of the LTC4314 ensures interoperability with noncompliant I²C devices that drive a high V_{OL} > 0.4V. This is shown in Figure 5 where a noncompliant device on channel 4 drives a high V_{OL} = 0.6V. The buffer turn-off voltage is 1.089V, yielding a logic low noise margin of > 0.4V at both the input and output.

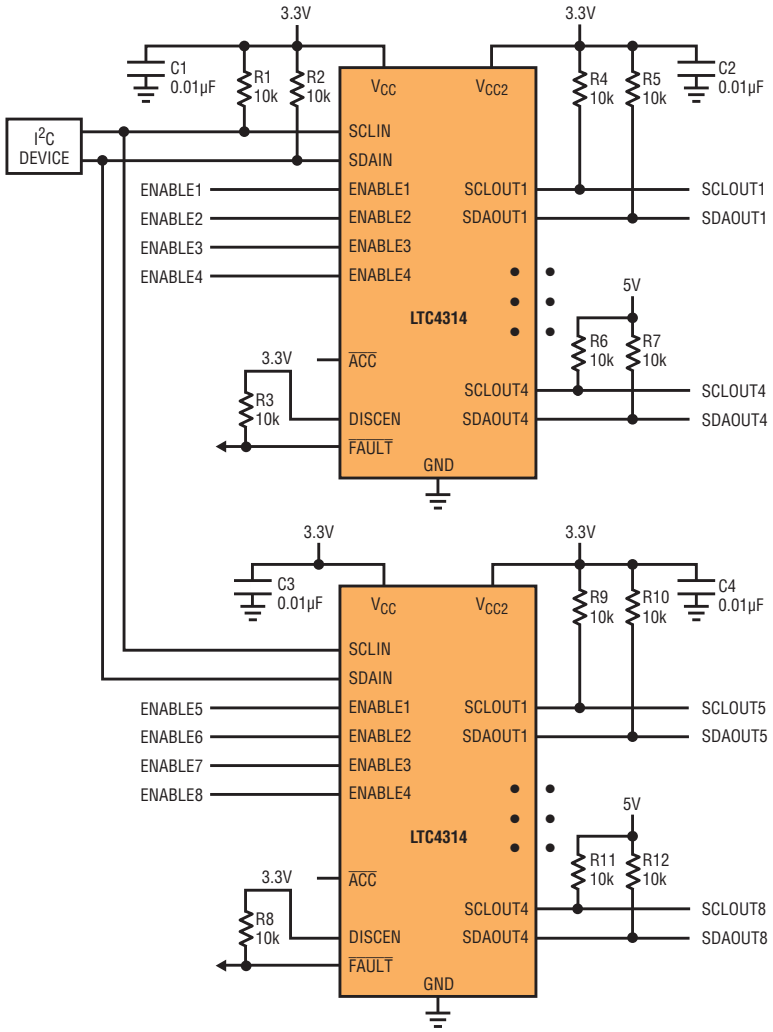


Figure 4. Paralleling LTC4314 devices to realize a 1:8 multiplexer

HOT SWAP™ APPLICATION

I/O cards can be hot swapped into the downstream buses of an LTC4314 residing on a live backplane as shown in Figure 6. Before plugging or unplugging an I/O card, care must be taken to disable the corresponding output channel so that the card does not disturb any I²C transaction that may be in progress. The connection to the inserted card must be enabled only when all ongoing transactions on the bus have completed and the bus is idle.

STUCK BUS DETECTION AND RECOVERY

Occasionally, slave devices get confused and get stuck in a low state. The LTC4314 monitors the enabled output buses to detect if clock and data have been simultaneously high at least once in 45ms. If this condition is not detected, the LTC4314 asserts the $\overline{\text{FAULT}}$ flag low. If DISCEN is tied high, the LTC4314 also disconnects the input and output sides and generates clock pulses on the enabled downstream buses in an attempt to free the stuck bus. Clocking is stopped when data releases high or 16 clocks have been generated, whichever comes first. After the final clock pulse, a stop bit is generated to reset the bus for further communication.

A rising edge on one or more ENABLE pins, after all ENABLEs have been taken low, is required to reestablish connection between the input and output. Doing this also clears the $\overline{\text{FAULT}}$ flag. The master can wait for the fault condition to clear ($\overline{\text{FAULT}}$ released high), either on its own or through the 16 clock pulses issued by the LTC4314, before toggling the LTC4314's ENABLE pins, or it can do so preemptively before the fault has cleared to reestablish connection. The master can then take appropriate action to clear the stuck low condition.

Figure 7 shows the waveforms during an SDAOUT1 stuck low and recovery event. After the 45ms timeout period has elapsed, the $\overline{\text{FAULT}}$ flag is asserted low and the input and output sides are disconnected. This causes SDAIN to release high.

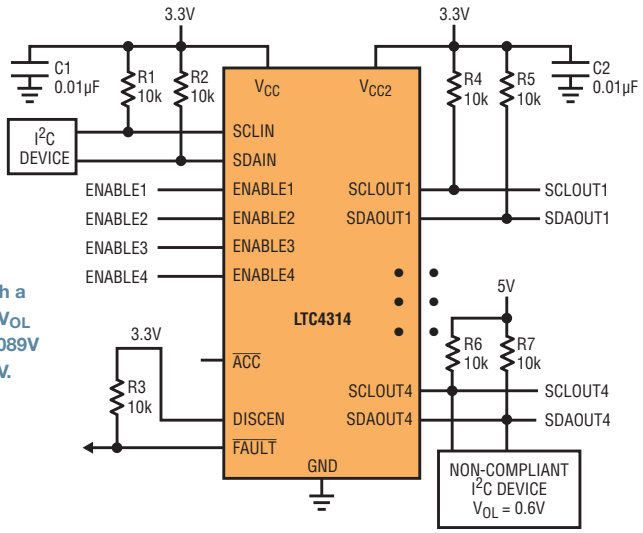


Figure 5. The LTC4314 in operation with a noncompliant I²C device that drives a V_{OL} = 0.6V. The buffer turn-off voltage is 1.089V yielding a logic low noise margin > 0.4V.

Table 2. $\overline{ACC}$ control of the rise time accelerator current I_{RTA} and buffer turn-off voltage $V_{IL,RISING}$(typ)

$\overline{ACC}$	I_{RTA}	$V_{RTA(TH)}$	$V_{IL,RISING}$
Low	Strong	0.8V	0.6V
Hi-Z	3mA	0.4 • V_{MIN}	0.33 • V_{MIN}
High	None	N/A	0.33 • V_{MIN}

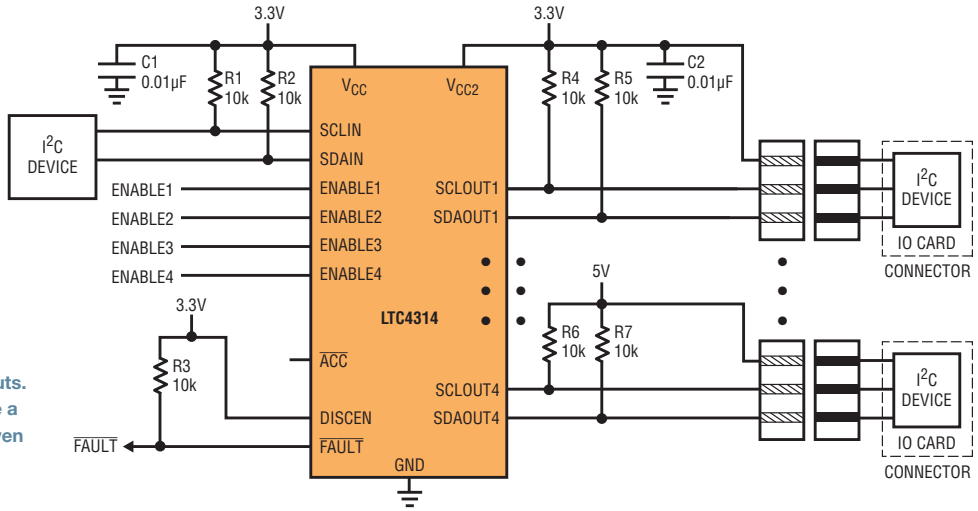


Figure 6. The LTC4314 in a Hot Swap™ application where cards are being plugged in to or unplugged from the outputs. The corresponding ENABLE pin must be driven low before a card can be plugged or unplugged and should only be driven high when the other buses are idle.

Clock pulses are generated on SCLOUT1. SDAOUT1 releases high before 16 clock pulses have been generated. Clock pulsing is stopped and a stop bit is generated. When the ENABLE1 pin is toggled, a connection is established between the input and output and a driven low level on SDAOUT1 is propagated to SDAIN.

If automatic stuck bus disconnection is not desired, this feature can be disabled by tying DISCEN low. In this case, during a stuck bus event, the $\overline{FAULT}$ flag is asserted low, but no stop bit or clock generation occurs and the input and output sides stay connected.

RISE TIME ACCELERATORS

The rise time accelerators (RTAs) of the LTC4314 can be configured either in current source mode ($\overline{ACC}$ open), slew limited switch mode ($\overline{ACC}$ grounded), or disabled ($\overline{ACC}$ high). In the current source mode the RTAs source a constant 3mA current into the bus. In the slew controlled switch mode, the RTAs turn on in a controlled manner and source current into the buses making them rise at a typical rate of 40V/µs. The RTA current and the buffer turn-off voltage are selected by the $\overline{ACC}$ setting as shown in Table 2.

For heavily capacitive buses with low to moderate noise, tie $\overline{ACC}$ low to meet system rise times and maximize SCL switching frequency. Tying $\overline{ACC}$ low provides the strongest pull-up current over the maximum voltage range. For higher noise immunity, leave $\overline{ACC}$ open or tie it to 0.5 • V_{CC} to set the buffer V_{IL} to 0.33 • V_{MIN} and to get 3mA of RTA current. The 3mA RTA current is enough to meet the 1µs standard mode I²C rise time requirement (100kHz operation) for bus capacitances up to 690pF with DC bus pull-up currents < 4mA. Tie $\overline{ACC}$ high if no acceleration is needed. To selectively disable RTAs only on the outputs, ground V_{CC2} and either ground $\overline{ACC}$ or leave $\overline{ACC}$ open.

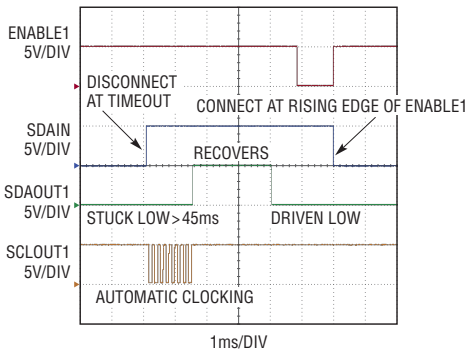


Figure 7. Bus waveforms during a SDAOUT1 stuck low and recovery event

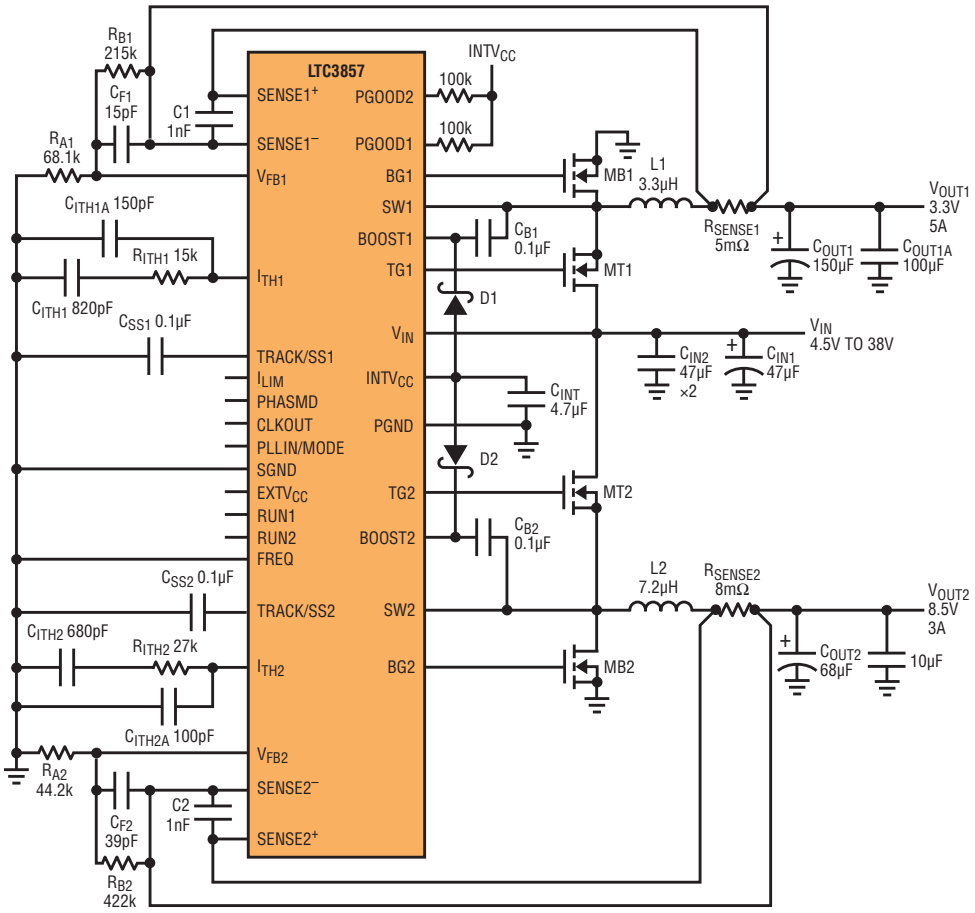
CONCLUSION

The LTC4314 and LTC4312 are pin-selectable I²C multiplexers that solve practical design issues associated with large I²C bus systems by providing capacitance buffering, nested addressing and level translation. These parts maintain a low offset and high logic low noise margin up to 0.33 • V_{CC}. Their high bandwidth buffers and integrated RTAs allow for operation at frequencies up to 1MHz with guaranteed stability from zero to 1.2nF capacitive loads. They also disconnect and recover buses when buses are stuck low and allow I/O cards to be hot swapped into and out of live systems. ■

Low I_Q, High Efficiency Dual Output Controllers for Wide Ranging Input and Output Voltages

Jason Leonard

The LTC3857 and LTC3858 are versatile low quiescent current (I_Q), 2-phase dual output synchronous buck controllers that are ideal for applications demanding high efficiency and minimal power loss over a broad range of load currents, from virtually no load to many amps. They feature a wide input supply range of 4V to 38V (40V abs max) that covers a broad range of battery chemistries and power sources. Each output can be set from 0.8V to 24V (28V abs max).



COUT1: SANYO 4TPE220MF
COUT1A: TAIYO YUDEN JMK325BJ107MM-T
COUT2: SANYO 10TPC68M

D1, D2: CENTRAL SEMI CMDSH-4E
L1: SUMIDA CDEP105NP-3R2MC-88
L2: SUMIDA CDEP105NP-7R2MC-88

MT1, MT2, MB1, MB2: INFINEON BSZ097NO4LS

The LTC3857 and LTC3858 are pin-compatible parts that differ only slightly, most notably in short-circuit operation and at light load operation. These differences are discussed below and summarized in Table 1. A "-1" version of each is available with slightly fewer features (Table 2). The LTC3857/LTC3858 are also mostly pin compatible with the popular LTC3827/LTC3826 family of low I_Q controllers. Figure 1 shows a typical application circuit in which the LTC3857 is used to convert a widely varying car battery voltage to two well regulated outputs.

LOW I_Q EXTENDS BATTERY RUN TIME

In many applications, one or more supplies remain active at all times, often in a standby mode where little or no load current is drawn. In these "always-on" systems, the quiescent current of the power supply circuit represents the vast majority of the current drawn from the input supply (battery). Having a low I_Q power supply is crucial to extending battery run times. In Burst Mode® operation, the LTC3857 draws only 50µA when one output is active and only 65µA when both outputs are enabled, while the LTC3858 draws 170µA when one output is active and only 300µA when both outputs are enabled. Both devices consume only 8µA when both outputs are shut down.

Figure 1. High efficiency dual output 3.3V/8.5V step-down converter. The 8.5V output follows V when V is less than 8.5V.

In "always-on" systems, the quiescent current of the power supply circuit represents the vast majority of the current drawn from the input supply (battery). Having a low I_Q power supply is crucial to extending battery run times.

Table 1. Key differences between the LTC3857 and LTC3858

FEATURE	LTC3857	LTC3858
Quiescent Current (One Channel On)	50µA	170µA
Quiescent Current (Both Channels On)	65µA	300µA
Burst Mode Operation	Lowest Ripple	Highest Midrange Efficiency
Short-Circuit Protection	Cycle-by-Cycle Current Limiting with Current Foldback	Cycle-by-Cycle Current Limiting with Current Foldback and Optional Short-Circuit Latchoff
Output Voltage Tracking During Start-Up	Yes, Tracking or Soft-Start (TRACK/SS Pin)	No, Soft-Start Only (SS Pin also Used for Short-Circuit Latchoff Timer)

OPERATING MODES

The PLLIN/MODE pin is used to program one of three modes at low load currents—Burst Mode operation, pulse-skipping mode, or forced continuous mode. Forced continuous mode maintains constant frequency operation from no load to full load, at the expense of light load efficiency. Burst Mode operation is the most efficient mode at light loads, albeit with slightly higher ripple and features the lowest quiescent current. Pulse-skipping mode is somewhat of a compromise, maintaining very low ripple and moderate efficiency at light loads. Figures 2 and 3 show the efficiencies in these three modes.

The LTC3857 and LTC3858 operate similarly to each other in forced continuous and pulse-skipping mode. There are differences in Burst Mode operation, however. The LTC3857 is optimized for the lowest quiescent current and for relatively low ripple. The LTC3858 is optimized for the highest efficiency over a broad range of load current. This means the LTC3857 transitions to constant frequency operation (with lower ripple) at a lower load current than the LTC3858, while the LTC3858 maintains higher efficiency (with higher ripple) at intermediate light loads (Figures 4 and 5).

CURRENT SENSING, CURRENT LIMIT AND SHORT-CIRCUIT PROTECTION

The LTC3857/LTC3858 each uses a peak current mode architecture. A high speed rail-to-rail differential current sense comparator constantly monitors the voltage across a current sense element, either a sense resistor or the inductor's DC resistance (as derived from an R-C network). The peak sense voltage is set by the three-state ILIM pin (fixed on the "-1" version). If a short circuit occurs, current limit foldback reduces the peak current to minimize the dissipation in the power components. Foldback is disabled during start-up for predictable tracking or soft-start.

The LTC3858 has an additional feature that further protects during a short-circuit event. The SS pin can be used as a short-circuit timer. If the short circuit lasts long enough, the output "latches off" and stops

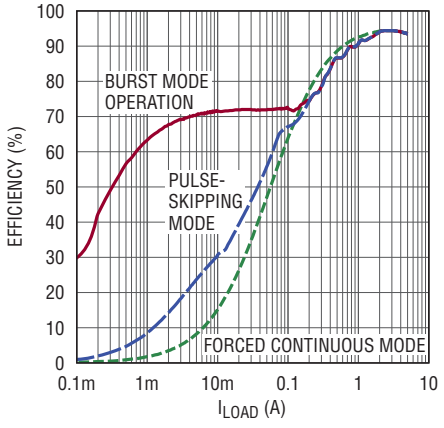


Figure 2. Efficiency of in the circuit of Figure 1 using the LTC3857. Efficiencies are shown for the three modes of operation (forced continuous, pulse-skipping, and Burst Mode operation). At heavier loads, the efficiency is independent of the mode.

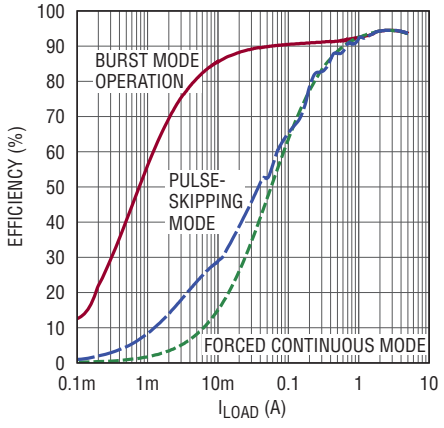


Figure 3. Efficiency of in the circuit of Figure 1 using the LTC3858. Note that the efficiencies in forced continuous and pulse-skipping modes are essentially identical to the LTC3857's in Figure 2—only Burst Mode operation is different at light to intermediate loads.

switching. The latch can only be reset by cycling the RUN pin or by cycling the input power (V_{IN}). This latchoff feature can be defeated by connecting a resistor between the SS and $INTV_{CC}$ pins. The two channels of the LTC3858 operate independently; i.e., a short-circuit latchoff on one channel does not affect the other channel.

Although both current foldback and latchoff provide additional levels of protection during a short-circuit event, the LTC3857/LTC3858 is fundamentally protected by its current mode architecture. The current comparator is always active, meaning switching cycles can be gracefully skipped as needed to keep the inductor current under control at all times.

OTHER IMPORTANT FEATURES

The FREQ pin is used to set the switching frequency. Tying this pin to ground selects 350kHz while tying it to $INTV_{CC}$ selects 535kHz. Connecting a single resistor from this pin to ground allows the frequency to be set anywhere from 50kHz to 900kHz. A short minimum on-time of 95ns allows low duty cycle operation even at high frequencies. The maximum 99% duty cycle capability allows low dropout operation for low input/high output voltage applications.

An internally compensated phase-locked loop (PLL) enables the LTC3857/LTC3858 to synchronize to an external clock source (applied to the PLLIN/MODE pin) from 75kHz to 850kHz. When synchronized, the LTC3857/LTC3858 operates in forced continuous mode to maintain constant frequency operation independent of the load current. When the external clock is absent or momentarily interrupted, the LTC3857/LTC3858 operates at the frequency set by the FREQ pin. The internal PLL filter is prebiased to a voltage corresponding to this free-running frequency. When an external clock is detected, the PLL is enabled. Since the PLL filter is prebiased and barely has to

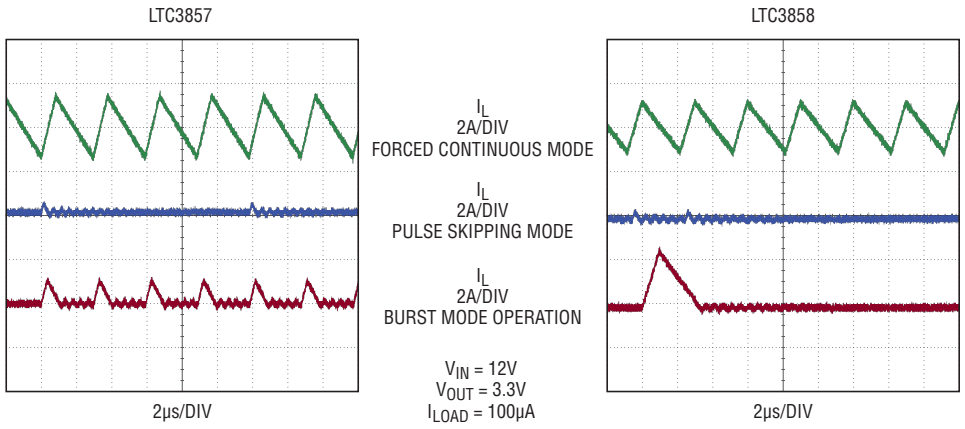
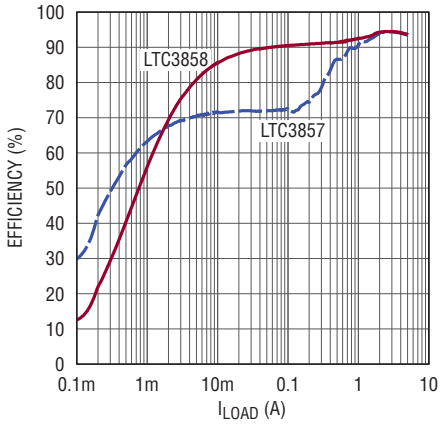


Figure 4. Inductor current ripple at 12V to 3.3V at 100µA load current. The LTC3857 and LTC3858 differ only in Burst Mode operation.

charge or discharge during this transition, synchronization is achieved quickly, with only small changes in frequency and minimal output voltage ripple.

The MOSFET drivers and control circuits are powered by $INTV_{CC}$, which by default is generated from an internal low dropout (LDO) regulator from the main input supply pin (V_{IN}). The strong gate drivers with optimized dead time control provide high efficiency at heavy loads. To reduce power dissipation due to MOSFET gate charge losses and improve efficiency at high input voltages, a supply between 5V and 14V (abs max) can be connected to

Figure 5. Comparison of the LTC3857 and LTC3858 efficiency when configured for Burst Mode operation (PLLIN/MODE pin connected to ground) for the Figure 1 circuit. At very light to virtually no load, the LTC3857 has the lowest power loss due to its low I_Q. At intermediate loads, the LTC3858 is more efficient, at the expense of ripple.



the $EXTV_{CC}$ pin. When a supply is detected on $EXTV_{CC}$, the V_{IN} LDO is disabled and another LDO between $EXTV_{CC}$ and $INTV_{CC}$ is enabled. $EXTV_{CC}$ is commonly connected to one of the output voltages generated by the LTC3857/LTC3858.

The LTC3857/LTC3858 features a RUN pin for each channel. RUN enables the output and the $INTV_{CC}$ supply. The LTC3857 has a TRACK/SS pin for each channel, which acts as a soft-start or allows the output to track an external reference (e.g., another supply). The LTC3858 has a dual-function SS pin for each channel. SS is used for soft-start (like the TRACK/SS pin on the LTC3857 but without tracking) and also as the optional short-circuit latchoff timer.

IDEAL FOR AUTOMOTIVE APPLICATIONS

The LTC3857, in particular, is well suited for automotive applications, including navigation, telematics and infotainment systems. The wide input voltage range is high enough to protect against double battery and load dump transients, while low enough to allow continuous operation during cold crank and engine start. The ultralow 50µA quiescent current is ideal for always-on supplies that are enabled even when the ignition is off. The wide output voltage range supports the higher voltage rails often used for audio systems, CD/DVD players, and disk

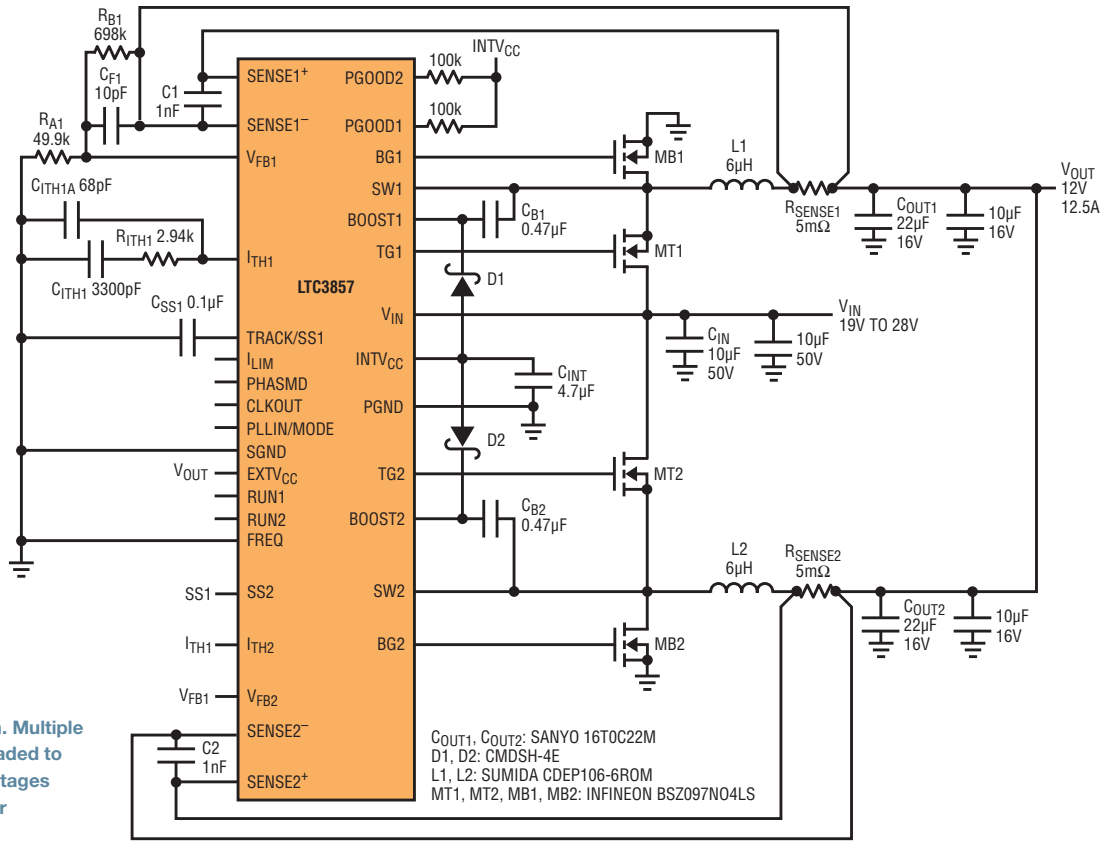


Figure 6. 2-phase single output application. Multiple LTC3857/LTC3858 controllers can be cascaded to drive a single output with up to 12 power stages operating out-of-phase for very high power applications.

drives. The 99% duty cycle capability provides a low dropout voltage for these rails when the battery voltage dips.

MULTIPHASE SINGLE OUTPUT APPLICATIONS

The LTC3857/LTC3858 is normally configured for two independent outputs that run 180° out-of-phase. Operating the channels out-of-phase minimizes the required input capacitance. However, the LTC3857/LTC3858 can also be configured with both power stages driving a single output. Figure 6 depicts a 19V–28V input supply generating a regulated 12V/150W output. In this configuration, both channels' compensation (ITH), feedback (V_{FB}), enable (RUN) and soft-start (TRACK/SS or SS) pins are tied together. Since the channels operate out-of-phase, the effective switching frequency is doubled, minimizing the required input and output capacitance and voltage ripple, while allowing for even faster transient response. The LTC3857/LTC3858 provides inherently fast, accurate cycle-by-cycle current sharing due to its peak current mode control architecture.

The LTC3857/LTC3858 can also be used in designs with three or more phases. The CLKOUT pin can drive the PLLIN/MODE pin of other controllers, while the PHASMD pin adjusts the relative phases of each controller. This allows 3-, 4-, 6- and 12-phase operation.

Table 2. Key differences between the standard and "-1" parts

	LTC3857/LTC3858	LTC3857-1/LTC3858-1
Current Sense Voltage	Adjustable 30mV/50mV/75mV (ILIM pin)	Fixed 50mV
Power Good Output Voltage Monitor	Independent Monitors for Each Channel (PGOOD1 and PGOOD2 pins)	Monitor for Channel 1 Only (PGOOD1 pin)
CLKOUT/PHASMD Pins for Three or More Phases	Yes	No
Package	5mm × 5mm QFN	28-Lead Narrow SSOP

CONCLUSION

The LTC3857 and LTC3858 are nearly pin-compatible parts, ideal for converters requiring high efficiency over a broad load range, from no load to full load. Their low quiescent current extends operating life in battery-powered systems. They each regulate two separate outputs from 0.8V to 24V from inputs of 4V to 38V. The short minimum on-time and 99% duty cycle capability allows high frequency operation from very low to very high duty cycles. The LTC3857 and LTC3858 incorporate these features and more in 5mm × 5mm QFN and 28-lead narrow SSOP packages. ■

High Efficiency Power Supply for Intel IMVP-6/IMVP-6+/IMVP-6.5 CPUs

Jian Li and Gina Le

The LTC3816 is a single-phase synchronous step-down DC/DC switching regulator controller that complies with Intel Mobile Voltage Positioning (IMVP)-6/6+/6.5 specifications. It uses a constant-frequency voltage mode architecture with a leading edge modulation topology, allowing extremely low output voltages and very fast load transient response. The LTC3816 satisfies all of the IMVP-6, IMVP-6+ and IMVP-6.5 requirements, including 7-bit VID code, start-up to a preset boot voltage, differential remote output voltage sensing with programmable active voltage positioning (AVP), I_{MON} output current reporting, power optimization during sleep state and fast or slow slew rate sleep state exit. It is suitable for a wide range of input voltages from 4.5V to 36V and output voltages up to 1.5V. The LTC3816 is available in 38-pin thermally enhanced eTSSOP and 5mm × 7mm QFN packages.

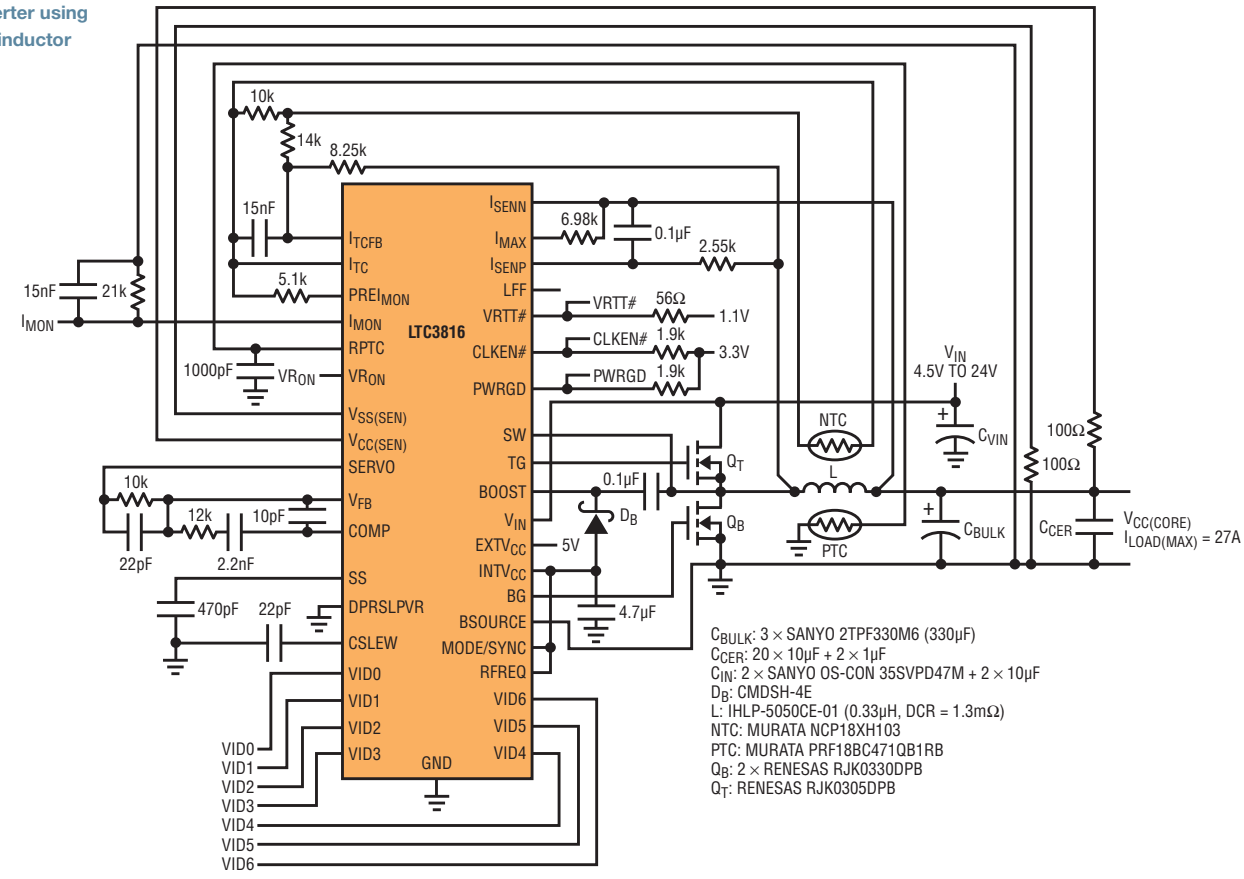


Figure 1. An IMVP-6.5 converter using temperature-compensated inductor DCR sensing

The LTC3816 meets all of Intel's IMVP-6, IMVP-6+ and IMVP-6.5 specifications in a small 5mm × 7mm 38-pin QFN. With strong gate drivers and short dead-time, the LTC3816 offers high efficiency solutions over a wide input voltage range. Its leading edge modulation topology allows very small duty cycle operation and ultrafast transient response.

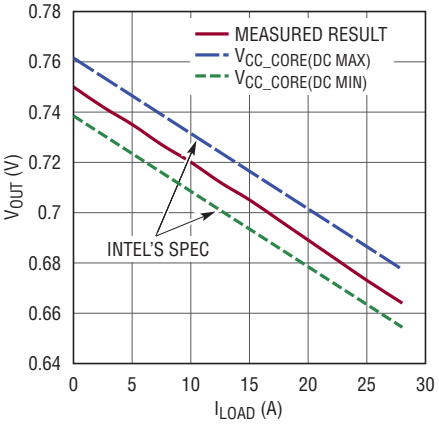


Figure 2. Load regulation with -3mV/A slope

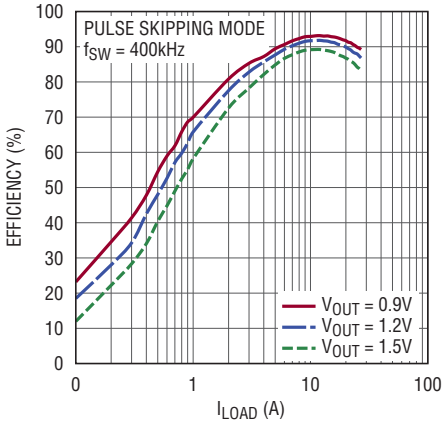


Figure 3. Efficiency with 12V input

AN IMVP-6.5 CONVERTER WITH 4.5V~24V INPUT AND 27A OUTPUT

Figure 1 shows an IMVP-6.5 application using temperature-compensated inductor DCR sensing. The output voltage is programmed by a 7-bit VID code. With temperature-compensated inductor DCR sensing, the LTC3816 provides an accurate –3mV/A AVP slope over temperature as shown in Figure 2. With strong integrated FET drivers and short dead-time, the LTC3816 offers a highly efficienct solution, as shown in Figure 3.

The LTC3816's leading edge modulation topology allows ultrafast transient response to meet Intel's stringent requirements. As shown in Figure 4, no undershoot other than AVP is observed during a load step-up test, easily meeting Intel's specifications. Moreover, the LTC3816 incorporates a line feedforward function to compensate for changes in the line voltage and to simplify the loop compensation. The LTC3816 feedback loop is also capable of dynamically changing the regulator output to different VID DAC voltages as shown in Figure 5. Upon receiving a new VID code, the LTC3816 regulates to its new potential with a programmable slew rate selected to prevent the converter from generating audible noise.

During start-up, the output voltage is charged to V_{BOOT} first, according to Intel's

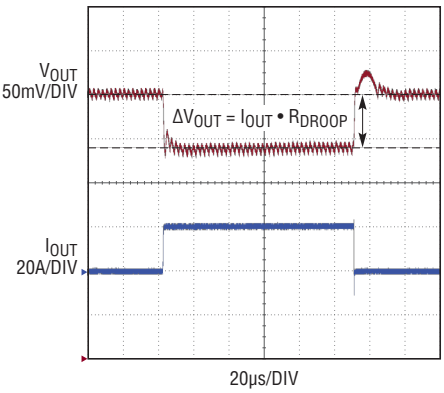


Figure 4. Transient response with 20A load step

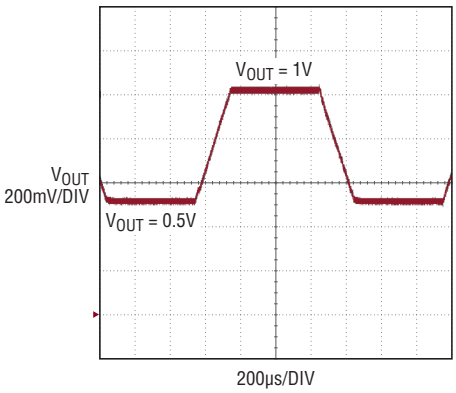


Figure 5. Output voltage transition from 0.5V to 1.0V in dynamic VID mode

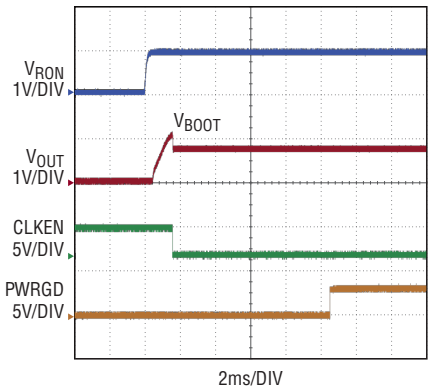


Figure 6. Start-up test with preset boot voltage 1.1V

The LTC3816 includes an onboard current limit circuit, so that the peak inductor current can be sensed via inductor DCR or a discrete sense resistor. The LTC3816 current limit architecture allows momentary overcurrent events for a predefined duration. The LTC3816 also provides input undervoltage lockout, output overvoltage protection and PWRGD and overtemperature flags.

IMVP specification. As shown in Figure 6, V_{BOOT} is 1.1V in IMVP-6.5 and 1.2V in IMVP-6. Once the output voltage reaches V_{BOOT}, the CLKEN# output goes low and the output voltage transitions to the voltage programmed by the VID code.

Figure 7 demonstrates that for high current applications, multiple LTC3816s can be paralleled to provide more power. The current sharing performance is very good in both static and dynamic operation conditions, as shown in Figure 8.

The LTC3816 includes an onboard current limit circuit, so that the peak inductor current can be sensed via inductor DCR or a discrete sense resistor. The LTC3816 current limit architecture allows momentary overcurrent events for a predefined duration. The LTC3816 also provides input undervoltage lockout, output overvoltage protection and PWRGD and overtemperature flags.

CONCLUSION

The LTC3816 meets all of Intel's IMVP-6, IMVP-6+ and IMVP-6.5 specifications in a small 5mm × 7mm 38-pin QFN. With strong gate drivers and short dead-time, the LTC3816 offers high efficiency solutions over a wide input voltage range. Its leading edge modulation topology allows very small duty cycle operation and ultrafast transient response. The LTC3816 provides high efficiency, high power density, and high reliability solutions for embedded computing, mobile computers, Internet devices and navigation displays. ■

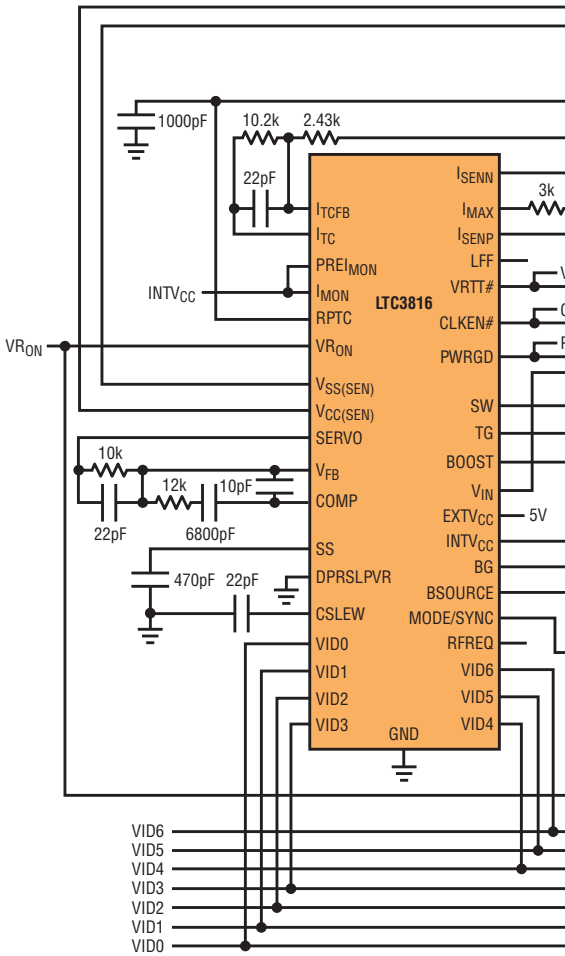
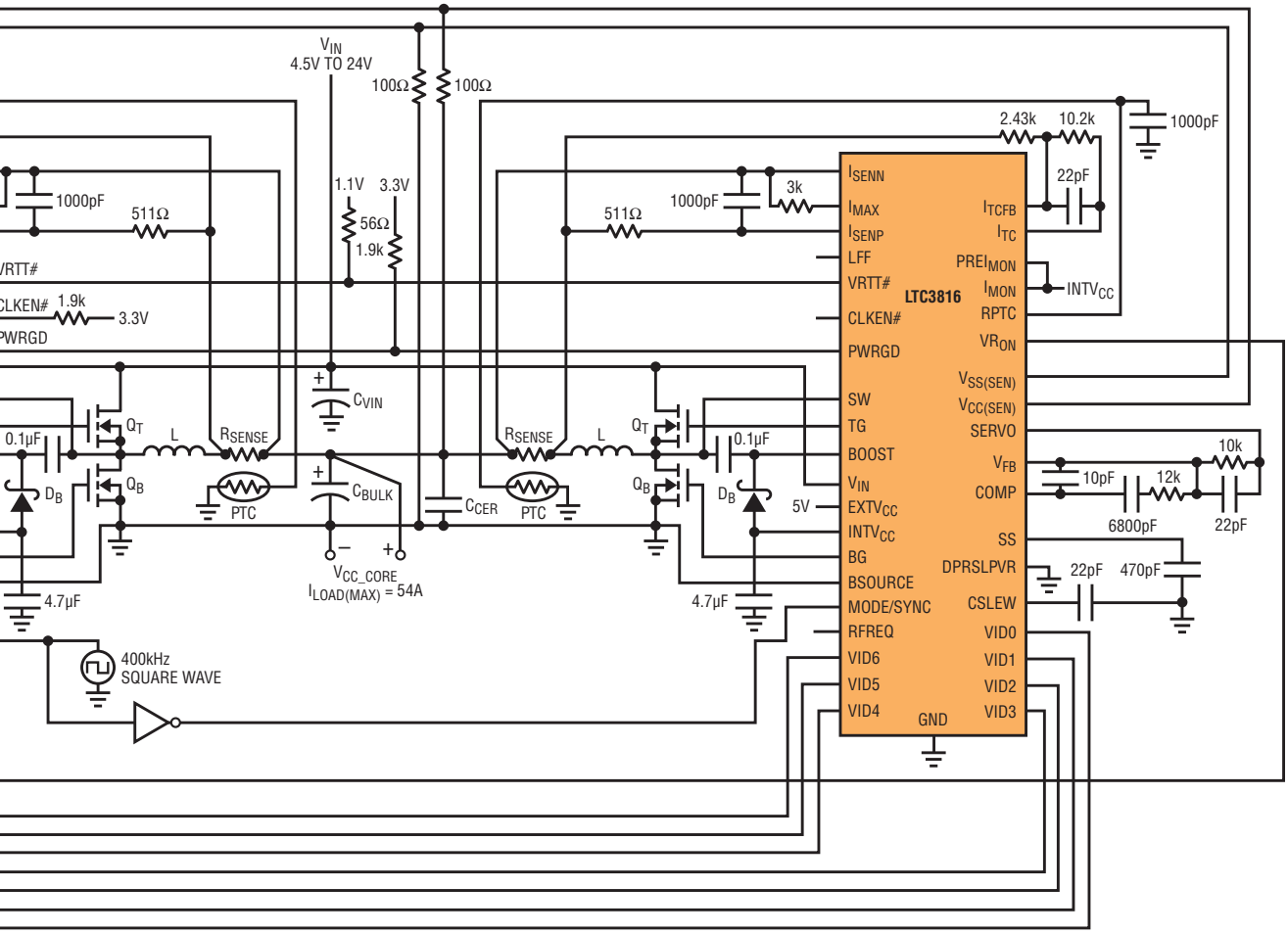


Figure 7. A dual-channel IMVP-6 converter with 44A output using R_{SENSE} sensing configuration

C_{BULK}: 4 × SANYO 2TPF330M6 (330µF)
C_{CER}: 32 × 10µF + 2 × 1µF
C_{IN}: 3 × SANYO OS-CON 35SVPD47M + 2 × 10µF
D_B: CMDSH-4E
L: IHLP-5050CE-01 (0.33µH, DCR = 1.3mΩ)
PTC: MURATA PRF18BC471QB1RB
Q_T: RENESAS RJK0305DPB
Q_B: 2 × RENESAS RJK0330DPB
R_{SENSE}: PANASONIC ERJM1WTF1M0U (1mΩ)

The LTC3816 feedback loop is also capable of dynamically changing the regulator output to different VID DAC voltages. Upon receiving a new VID code, the LTC3816 regulates to its new potential with a programmable slew rate selected to prevent the converter from generating audible noise.



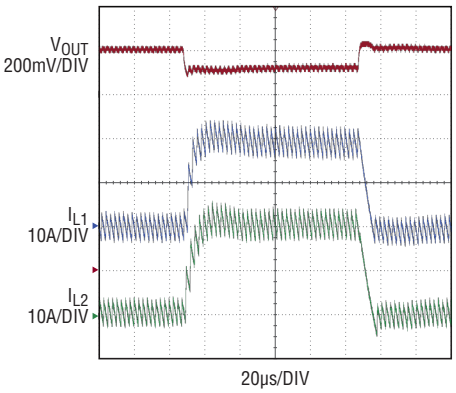


Figure 8. Current sharing performance for a dual-channel IMVP-6 converter

3A Linear Regulator Can Be Easily Paralleled to Spread Power and Heat

Todd Owen

The basic 3-terminal regulator has been a building block in designer tool kits for over thirty years without any significant change to its basic architecture. Using a fixed voltage reference, a resistor divider boosts the output voltage to the desired level. These are easy to use devices, hence their popularity, but there are some inherent downsides to this simple architecture.

One drawback to using a traditional linear regulator is that the minimum output voltage is limited to the reference voltage of the regulator. Another is that it is not easy to increase the available output current or spread power dissipation by paralleling devices. To distribute the load between multiple regulators, one must either add large ballast resistors, which incur load regulation errors, or balance the load with complicated schemes of input sense resistors and op amp loops, which inevitably cancels out the promise of simplicity originally offered by using the ostensibly simple linear regulator.

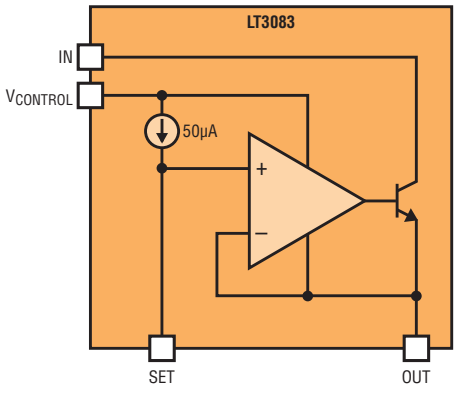


Figure 1. LT3083 block diagram

But what if the voltage reference is thrown out and replaced with a precision current source? The resulting device is deceptively simple, as shown in the block diagram of Figure 1; a precision current source connects to the noninverting input of an amplifier and the output drives a large NPN pass element and connects to the inverting input to give unity gain. This small change to the venerable linear regulator device yields enormous gains in versatility and performance.

Now, in this new architecture, connecting each of the SET pins together when paralleling regulators provides a common reference point for *all* the error amplifiers, making it possible to balance any device-to-device offset variations with mere milliohms of ballast. Suddenly it is easy to spread power dissipation between as many devices are needed, and likewise scale the output current as necessary. The beauty of this architecture is that a single resistor generates the reference point for all of the regulators, whether one, ten or one hundred regulators are used. Additionally, the architecture allows zero resistance to equal zero output—there is no longer a fixed reference voltage to limit the bottom end of the usable output voltage range.

BENEFITS OF A NEW ARCHITECTURE

The LT®3080 1.1A linear regulator was the first linear regulator to use a precision current source architecture, making it possible to produce high current, surface mount power supplies by paralleling any number of LT3080s. The LT3083 follows in the footsteps of the LT3080 with similar high performance specifications, but with an increased 3A output current capability. The performance advantages offered by this new architecture are numerous.

Frequency Response and Load Regulation are Fixed

With traditional linear regulators, gain and bandwidth change as the output voltage is changed via resistor divider. Bypassing the feedback pin of the regulator affects loop response. Load regulation is not a fixed value, but a fixed percentage of the output as the resistor divider gains up any voltage deviation. Furthermore, reference voltage noise is gained up by the same resistor divider.

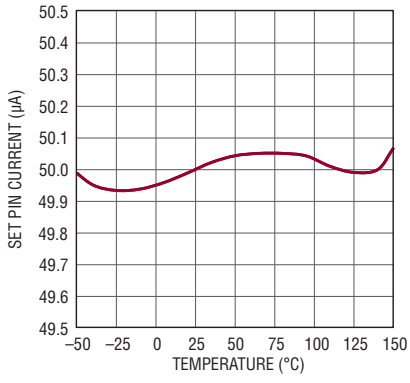


Figure 2. Reference current temperature characteristics

Suddenly it is easy to spread power dissipation between as many devices are needed, and likewise scale the output current as necessary. The beauty of this architecture is that a single resistor generates the reference point for all of the regulators, whether one, ten or one hundred regulators are used.

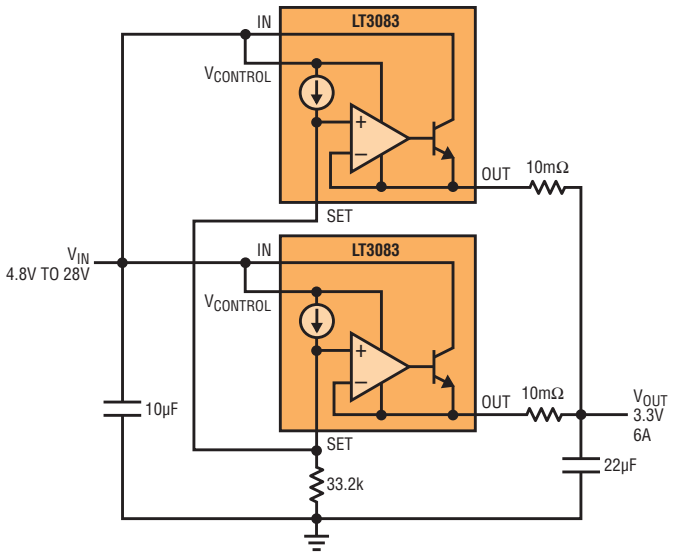


Figure 3. Paralleling regulators for higher current and heat spreading

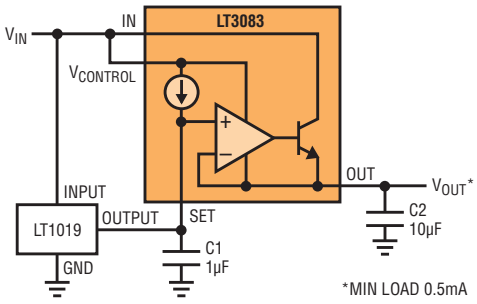
Using a current source and unity-gain buffer eliminates these downsides. Since the error amplifier is always in unity gain, frequency response does not change as a function of output voltage or with the use of bypassing across the reference point. Load regulation is now a fixed value, regardless of output voltage. Since bypassing does not affect loop response, two noise sources can be eliminated: the reference current noise and resistor shot noise are quieted using a single capacitor. This leaves only the error amplifier noise at the output, and again, that stays at a fixed level, no matter the output voltage.

Top Notch DC Characteristics

DC characteristics of the LT3083 are the same as the original LT3080. The LT3083 separates out the collector of the NPN pass device to minimize power dissipation. Load regulation is typically below 1mV for the error amplifier, and nearly immeasurable on the 50µA reference current. Line regulation for the reference current is less than 0.0002%/V, and is typically 2µV/V for the error amplifier offset. Temperature characteristics of the reference current are excellent, typically staying within 0.2% across the full operating junction temperature range, as shown in Figure 2.

The LT3083 also provides all of the protection features that Linear Technology parts are known for: current limit with safe operating area protection protects the device from damage during short-circuit conditions and thermal limiting keeps the part safe during conditions of excessive power dissipation.

Figure 4. High current reference buffer



Top Notch AC Characteristics

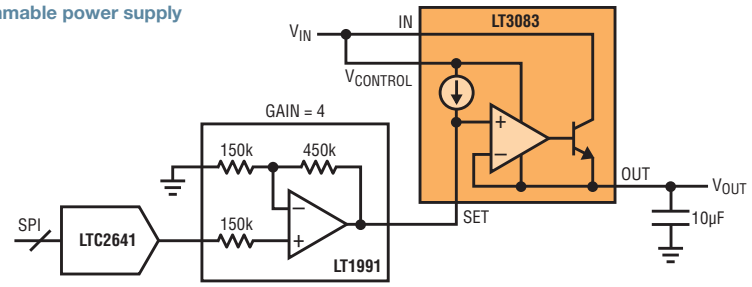
Don't think that the AC characteristics of the LTC3083 were sacrificed in an effort to achieve high DC performance. Transient response is excellent with as little as 10µF of output capacitance. Small ceramic capacitors can be used without the addition of ESR. Using a bypass capacitor across the reference resistor provides a slow-start function; the output voltage follows the RC time constant created by the SET resistor and bypass capacitor. Paralleling devices also provides advantages in noise performance. Paralleling multiple LT3083 regulators lowers the output noise in the same way that paralleling n op amps lowers noise by a factor of $\sqrt{n}$.

APPLICATIONS

The LT3083's deceptively simple architecture and high performance parameters make it powerful building block for applications beyond the basic linear regulator. It can be easily paralleled to increase output current and spread heat. Actively driving the SET pin is perfectly acceptable; the low offset and high output current allow for highly accurate reference supplies at high power levels. Digitally programmable supplies are achieved by driving the SET pin with a DAC. Accurate current sources are realized without tremendous difficulty. The possibilities are only limited by the creativity of the user.

The LT3083 is easily configured as a 2-terminal current source, simply by adjusting the ratio of the external resistors and adding compensation.

Figure 5. Digitally programmable power supply



Parallel Regulators Increase Current and Spread Heat

Figure 3 shows how to parallel multiple LT3083s to increase output current and spread heat. Note the minimal ballast needed to balance the load amongst the regulators. It's possible to produce quiet and accurate high current surface mount supplies simply by adding more LT3083s. Power dissipation is spread evenly across the paralleled regulators, but thermal management is still necessary. With as little as 0.5V drop across the regulator, a 3A load translates to 1.5W of power dissipation, pushing the thermal capabilities for surface mount designs.

High Current Reference Buffer

Creating a high current reference buffer takes very little effort, as shown in Figure 4. In this circuit, an LT1019-5 output connects to sink the 50µA reference current of the regulator. This reference provides 0.2% accuracy across temperature, or 10mV. With a maximum offset voltage of 4mV in the LT3083, output accuracy stays within 0.3%. The accuracy of the reference current in the LT3083 is not a factor in the output tolerance, and there are no resistors to present potential tolerance variations.

Digitally Programmed Output

Programming the output voltage digitally simply takes the addition of a DAC to drive the SET pin. Figure 4 highlights how a DAC programs the LT3083 output to anywhere from zero to over 16V within 1.5LSB. In this circuit, an LTC2641-12 using a 4.096V reference drives the SET pin of the LT3083 through the LT1991 (configured for a gain of four).

Again, the tight specifications of the LT3083 allow for such excellent performance. Keep in mind that the minimum load current requirement must be met when operating at minimum output voltages—less than 500µA loading is required when operating at low input voltages, much less than traditional linear regulators that require 5 to 10mA.

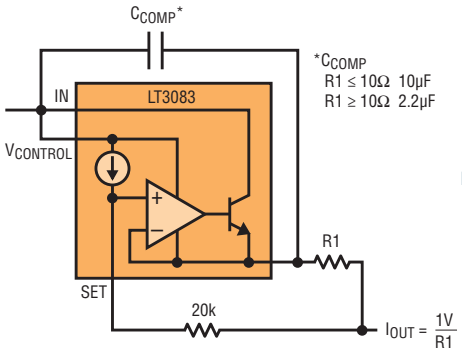


Figure 6. 2-terminal current source

Easy 2-Terminal Current Source

Current sources can be very difficult to implement in certain applications. Some must be ground referenced, others must be referenced to a positive rail, while the most difficult designs require floating, 2-terminal devices. The LT3083 is easily configured as a 2-terminal current source, simply by adjusting the ratio of the external resistors and adding compensation as shown in Figure 5. The current source can be ground referenced, referenced to a positive rail or fully floating without concern.

CONCLUSION

Hiding behind the simple architecture shown in the block diagram of the LT3083 is a high performance, highly versatile, groundbreaking building block device. The LT3083 combines the architectural leap forward of the LT3080, excellent AC and DC characteristics and increased current to easily solve problems that a traditional 3-terminal or low dropout regulator cannot touch. It can be used for supplies that operate all the way down to zero volts, paralleled for high current and heat spreading, or driven dynamically. High current linear power supplies are now available for surface mount boards without sacrificing performance. ■

8-Output Regulator Powers Applications Processors

Kevin Ohlson

The market for applications processors, the integrated core/memory/video/UI function chips used in smartphones, tablets, netbooks and automobile infotainment systems, is one of the fastest growing segments in electronics today. A single applications processor IC, such as one from Freescale, Marvell or an in-house custom processor, is packed with functions and requires independent power supplies for its core, I/O, memory and peripherals. The challenge is producing all those rails in limited space, at high efficiency, from a wide range of power inputs—a tablet, for instance, requires power conversion from USB, automotive battery and its built-in Li-ion battery.

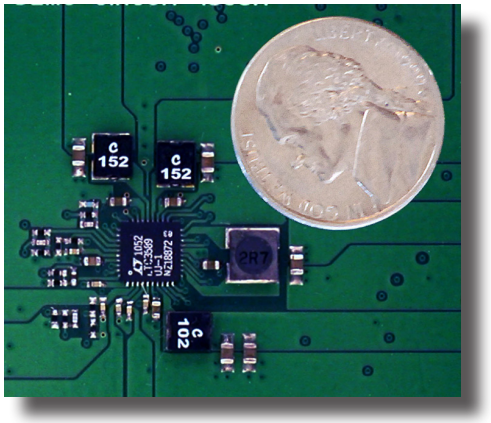


Figure 1. Eight power rails take less than 500mm² of board real estate.

The LTC3589 serves applications processor power needs with eight regulated outputs that support processor core and I/O voltage levels, SRAM, memory, low power standby, other peripheral circuits and system voltage levels. The LTC3589's eight supplies are completely independent, but they can be easily sequenced with simple pin strapping. Likewise, the LTC3589 simplifies overall power system design by integrating a number of important control features, including:

- Flexible pin strap supply sequencing
- I²C control of all major regulator functions
- Dynamic voltage scaling with selectable ramp rate
- IRQ pin and status register error reporting
- Power good status pin and register
- Built-in pushbutton controller to initiate power-on, provide a debounced pushbutton status and force a device hard reset

EIGHT INDEPENDENT VOLTAGE REGULATORS IN A SINGLE IC

While the features built into the LTC3589 certainly aid system design and optimization, it is designed foremost to output eight independent, voltage-regulated outputs. The LTC3589 contains a combination of LDO and switching regulators with output current capabilities from 25mA to 1.6A, with voltage output levels from less than 1V to 5V. Four of the outputs feature I²C -controlled DAC references for dynamic voltage scaling.

The integrated low power, 25mA, LDO can supply circuits that require a constant supply while the system is in standby mode, such as a real time clock. The low power LDO is capable of producing an output from 0.8V up to the input

Table 1. The LTC3589 supplies eight voltage rails delivering currents from 25mA to 1.6A

TYPE	AVAILABLE OUTPUT CURRENT	OUTPUT VOLTAGE CONTROL
LDO1	25mA	Resistive divider based on 0.8V feedback reference
LDO2	250mA	Resistive divider based on 0.3625V to 0.75V DAC feedback reference
LDO3	250mA	Fixed 1.8V
LDO4	250mA	1.8V, 2.5V, 2.8V, 3.3V selectable using I²C command register
Buck1	1.6A	Resistive divider based on 0.3625V to 0.75V DAC feedback reference
Buck2	1A	Resistive divider based on 0.3625V to 0.75V DAC feedback reference
Buck3	1A	Resistive divider based on 0.3625V to 0.75V DAC feedback reference
Buck-Boost	1.2A	Resistive divider based on 0.8V feedback reference

The LTC3589's eight supplies are completely independent, but they can be easily sequenced with simple pin strapping. Likewise, the LTC3589 simplifies overall power system design by integrating a number of important control features.

supply, set by a resistive divider. As long as an input supply is attached to the LTC3589, the always-alive LDO regulates. The LTC3589 only consumes 8µA of input supply current in standby mode, even as the always-alive LDO regulates.

Three more LDOs, each capable of delivering 250mA, are handy for supplying power to system analog functions such as phase lock loops, D/A and A/D converters, or as general purpose rails. The 250mA LDO regulators can be powered from a voltage lower than the primary input supply to reduce the power consumption in the LDO. Typically, the LTC3589 switching converters supply the LDO regulators. Two of the LDO regulators have fixed or I²C selectable output voltage. The third LDO uses external feedback resistors with a 5-bit DAC reference to set its output using an I²C command register.

The LTC3589 is designed to run from an input supply range of 2.7V to 5.5V. To satisfy the requirements of devices that require a 3.3V or 5V rail, the LTC3589 includes a high efficiency buck-boost switching converter that can output voltage from 1.8V to 5V, set by a resistive divider. The buck-boost converter is capable of supporting loads up to 1.2A. Using the I²C serial port, the buck-boost converter can be set to low power Burst Mode operation to reduce power loss in low current output modes.

Three buck regulators complete the LTC3589 complement of regulated

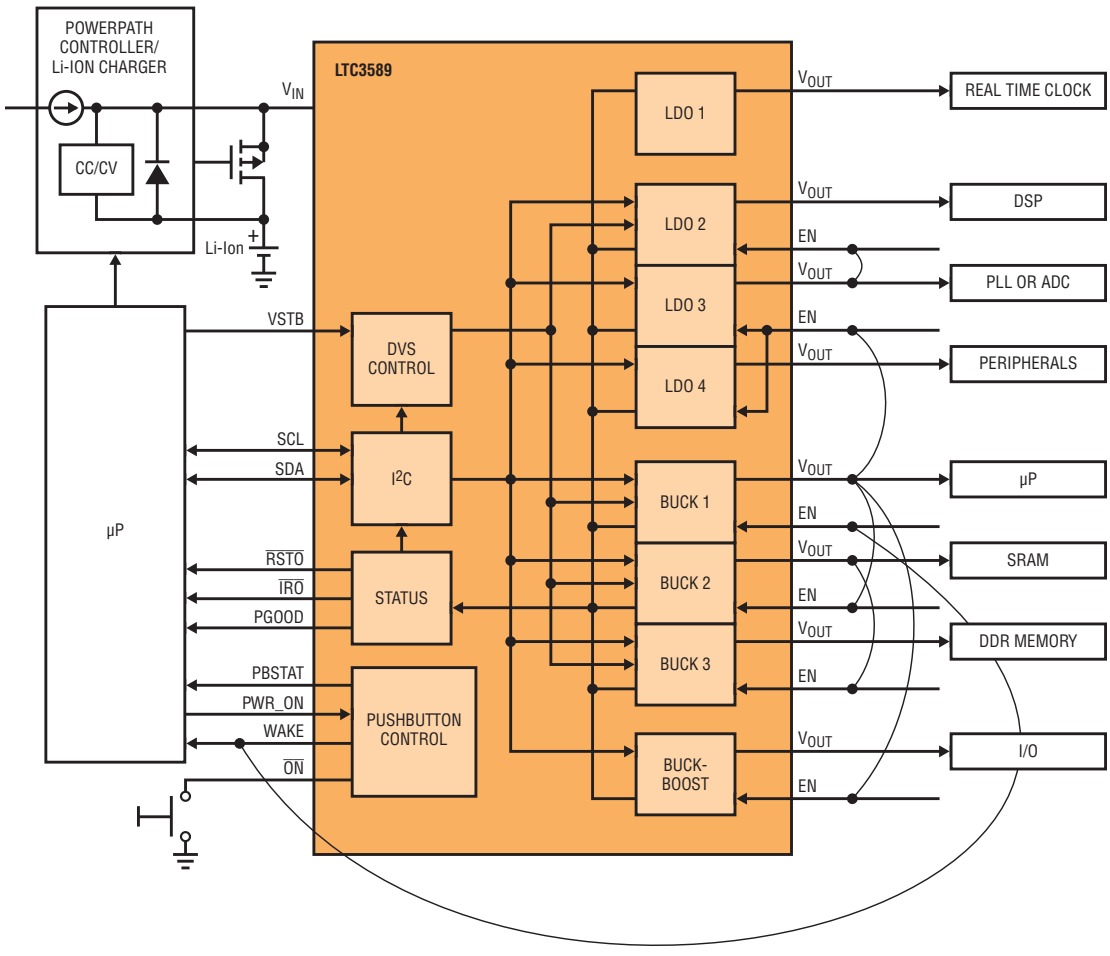
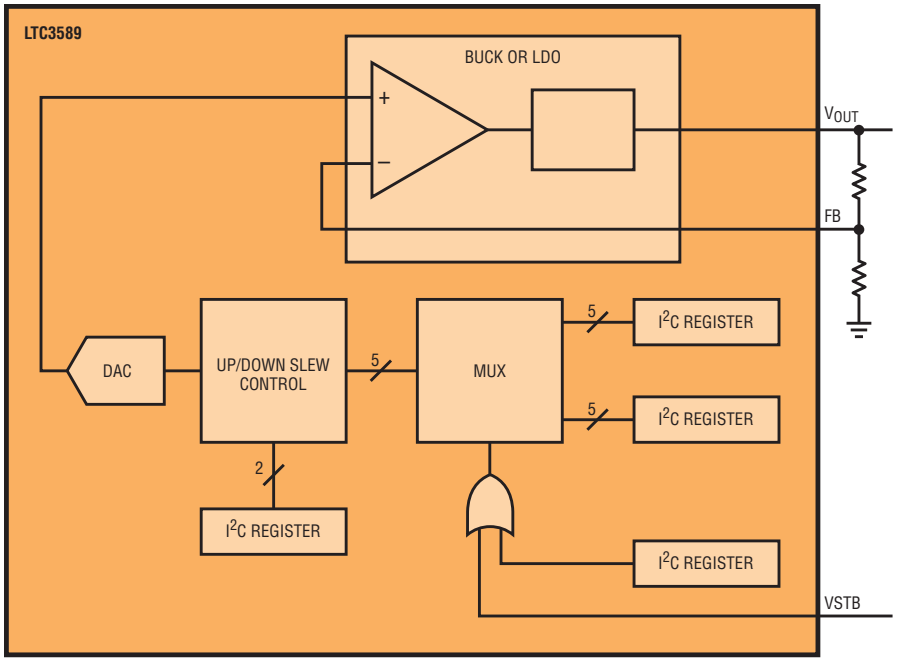


Figure 2. Combine the LTC3589 with a PowerPath™ controller/battery charger for power distribution with supply sequencing, I²C controls and pushbutton control.



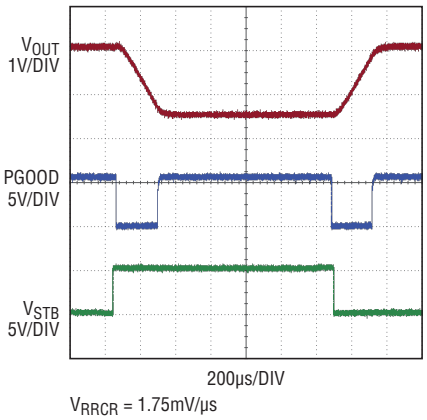


Figure 3. Dynamic voltage scaling is supported on four of the LTC3589's eight outputs with I²C selectable up/down slew rate.

voltage outputs. The buck converters' output voltages, set with external resistor dividers, can range from as low as the minimum DAC reference voltage to as high as the input supply voltage, where the bucks operate in dropout mode.

Depending on the requirements of the application, each buck's operating mode can be set using the I²C command registers. For operation over a wide range of output currents, pulse-skipping mode gives good efficiency with low ripple. Burst Mode operation offers the highest efficiency at low power. When set to Burst Mode operation, the buck automatically moves between Burst Mode operation at low loads and continuous switching mode at higher output loads. Selecting forced continuous mode results in the lowest output voltage ripple at the expense of some efficiency. Each buck's operating mode is independently selected using the I²C command registers.

DYNAMIC VOLTAGE SCALING

Since portable battery operated devices spend much of the time in standby or low power modes, microprocessors may take advantage of dynamic voltage scaling to reduce switching power loss by decreasing the processors supply voltage. The LTC3589 supports dynamic voltage scaling (DVS) on one of the LDO regulators and all three buck converters.

Each scalable regulator on the LTC3589 uses two DAC feedback reference set-point voltages in the I²C command registers and a selectable transition slew rate between the high and low target voltages (see Figure 3). Transition between target voltages is initiated for all regulators using the VSTBY pin or for individual regulators using I²C command registers.

The scalable LDO and buck converters have independently controlled DAC-driven feedback reference voltages. The reference voltage range runs from 0.3625V to 0.75V in 31 12.5mV steps. The converter output voltage is scaled up from the reference voltage using a resistive feedback divider from the converter output to its feedback input. At power-on, each DAC defaults to a reference output of 0.675V so the output voltage can be increased from the default output by 10% to increase the processor performance or for power supply margining.

During a voltage-down slew, the step-down regulators are automatically switched to forced continuous mode and therefore are able to sink current from the load. A 2k resistor to ground is switched to the output of the DAC-referenced LDO to pull down its output. Four slew rates are selectable by choosing the rate of change of the reference, from 0.88V/ms to 7V/ms, via the I²C command register.

EASY SEQUENCING AND ENABLE CONTROL

Multirail systems typically require the supply rails come up to voltage in a predetermined sequence (because of latchup, brains in right order, start-up current, etc.). Sequencing the LTC3589 outputs in any order is accomplished by pin-strapping regulator outputs to regulator inputs. Figure 4 shows an example of a pin-strapped sequence. Each enable pin has a precise 500mV comparator input with a built-in 200µs delay timer before enabling the regulator.

The start-up sequence is defined by tying the LTC3589 WAKE pin to the enable pin of the first regulator or regulators in the sequence. Wrapping regulator outputs around to the next enable in the

A regulator not in the start-up sequence is controlled by driving its pin directly or using the I²C command register. Any of the regulators in a pin-strapped sequence can be enabled or disabled in any order by setting a software control bit in the I²C command registers.

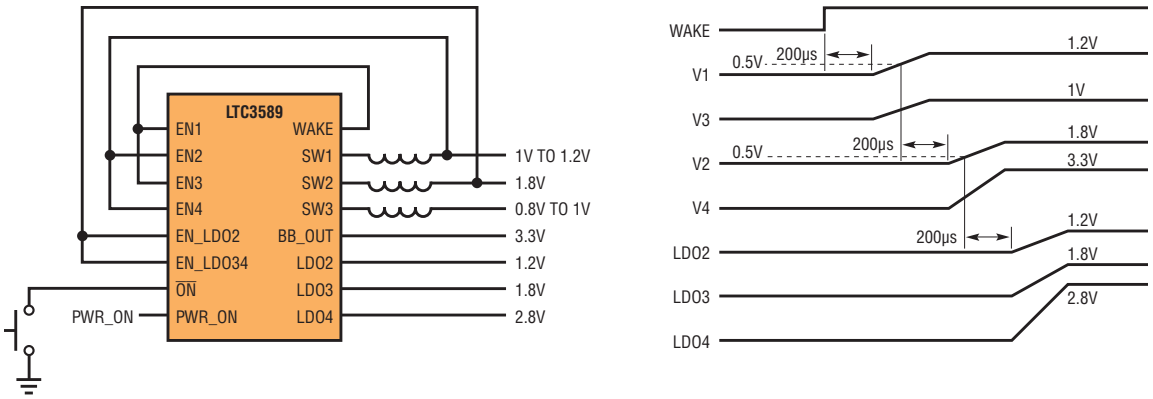


Figure 4. Flexible and simple start-up sequencing is accomplished by tying regulator outputs to enable pins in any order.

sequence brings the supplies up in order. If additional start-up delay is required, add a resistive divider to raise the enable voltage threshold or add an RC filter with the desired time constant to delay the start of the subsequent regulator.

A regulator not in the start-up sequence is controlled by driving its pin directly or using the I²C command register. Any of the regulators in a pin-strapped sequence can be enabled or disabled in any order by setting a software control bit in the I²C command registers. Once the software control bit is set, all the regulators ignore their enable pin status and respond only to I²C command register control. This allows a regulator to be powered down without affecting the subsequent regulators in a pin-strapped sequence.

Applications with keep-alive requirements such as volatile memory or watchdog functions requiring more power or additional voltage rails can take advantage of the LTC3589 keep-alive control function. Each of the three buck converters and the DAC-controlled LDO have a keep-alive bit setting in the I²C control register. Setting any of the keep-alive bits in the I²C command register keeps the corresponding regulators alive when the LTC3589 is in standby mode.

To ensure the integrity of a power-up sequence following a power-down, the LTC3589 adds a one second delay to allow the regulator outputs to fall to ground. Additionally, 2k pull-down resistors are inserted on the LDO outputs and buck switch pins to ensure discharge. Each regulator's output voltage must be less than 300mV before it is allowed to enable. I²C command register settings are available to override the resistor pull-downs and the 300mV start-up rule in cases where the regulator outputs are back-driven.

PUSHBUTTON OPERATION

The pushbutton control circuit included in the LTC3589 provides a debounced user interface to initiate a power-up sequence. A power-up sequence from standby mode begins when the pushbutton is depressed to activate the open driver WAKE pin. If the WAKE pin is tied to a regulator enable pin, the power-up sequence begins. Once the controller is satisfied system power is good then the PWR_ON pin should be driven high. For normal shutdown, pull PWR_ON low.

The PBSTAT pin is an open drain output that signals to the microprocessor that the button has been pushed and some change in operation or power-down has been requested. If the system is no longer responding for some reason, holding the button for five seconds forces a hard reset, which powers down the regulators, asserts the $\overline{\text{RSTO}}$ reset pin and puts the LTC3589 in standby mode.

If pushbutton functions are not needed, the WAKE pin is enabled and disabled by driving the PWR_ON pin directly. Even when driving the PWR_ON pin directly, the pushbutton PBSTAT status pin and hard reset functions are active.

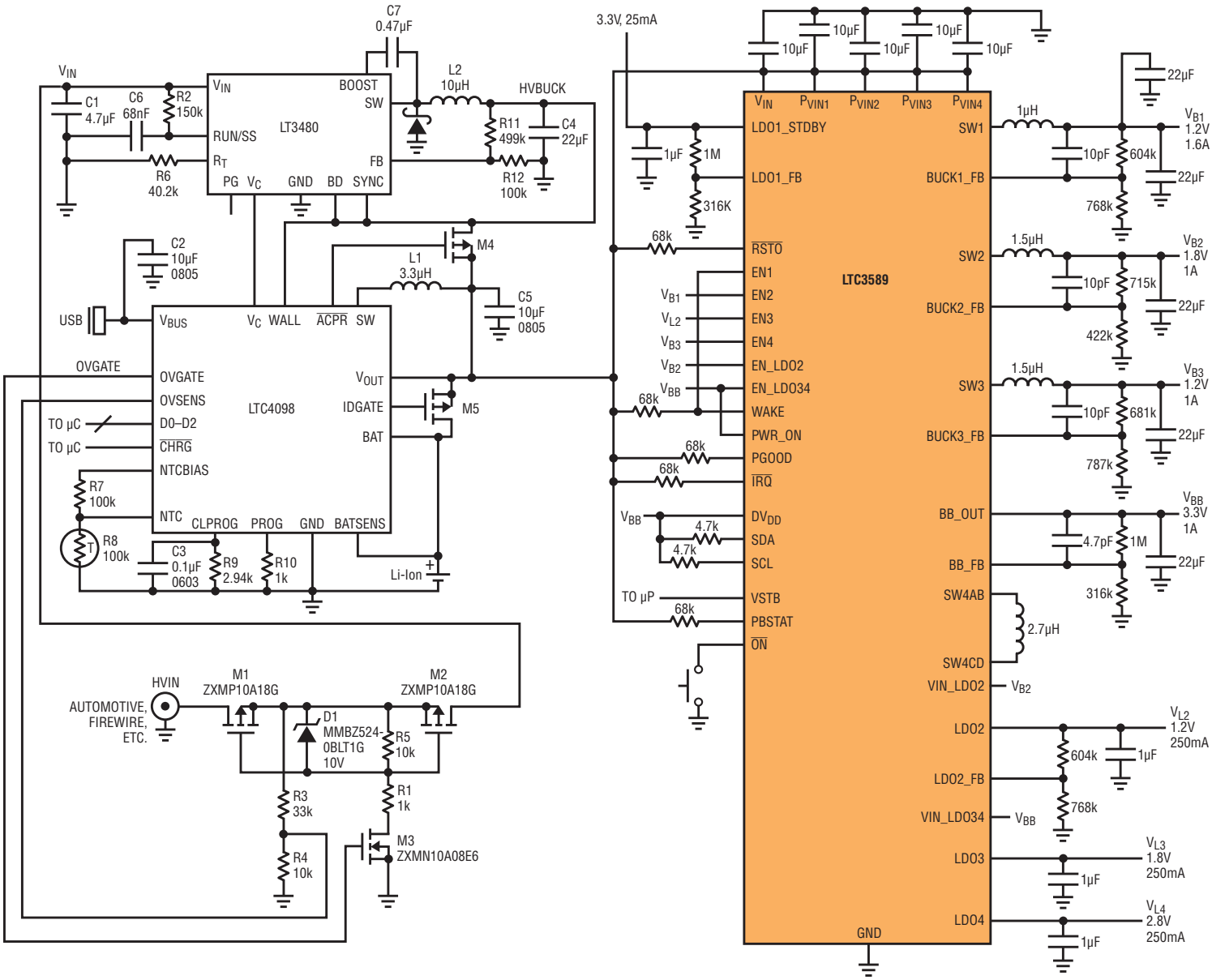


Figure 5. Integrated power IC for mobile microprocessor system with USB/automotive battery charger

STATUS REPORTING

Three pins are provided for the LTC3589 to send status to the controlling microprocessor. The $\overline{\text{RSTO}}$, $\overline{\text{IRQ}}$, and PGOOD pins are open drain outputs that signal regulator low output, hard reset events, supply undervoltage, hot die temperature and fault conditions. The $\overline{\text{IRQ}}$ and PGOOD pins are matched to I²C status registers, which can be read to determine the specific cause of the status pin activity. In the event of a fault, such as die overtemperature or UVLO, that shuts down the LC3589 regulators, the cause of the shutdown is latched in a status register that can be read by the system controller after system reboot.

CONCLUSION

The LTC3589 with eight regulator outputs, flexible sequencing, dynamic voltage scaling and serial port control is ideally suited for applications-processor-based consumer, industrial and automotive devices. When coupled with a step-down regulator, the LTC3589 can supply a complete set of system supply rails from high voltage primary sources such as automotive systems. Add a PowerPath controller/battery charger IC to generate system rails for Li-ion-powered portable devices.

The LTC3589 features low power standby and Burst Mode operation, keep-alive functions and dynamic voltage scaling so that system designers can optimize battery life. Pushbutton control simplifies board design and provides start-up, processor interrupt and hard reset functions. ■

3-Phase Synchronous Step-Down DC/DC Controller with Stage Shedding, Active Voltage Positioning and Nonlinear Control for High Efficiency and Fast Transient Response

Jian Li and Kerry Holliday

The LTC3829 is a feature-rich single-output 3-phase synchronous buck controller with on-chip drivers, remote output voltage sensing, inductor DCR temperature compensation, Stage Shedding™ mode, active voltage positioning (AVP) and nonlinear control. It is suitable for input from 4.5V to 38V and output from 0.6V up to 5V. The LTC3829 provides high efficiency, high power density and versatile power solutions for computers, telecom systems, industrial equipment and DC power distribution systems. The LTC3829 is available in 38-pin 5mm × 7mm QFN and 38-pin FE packages.

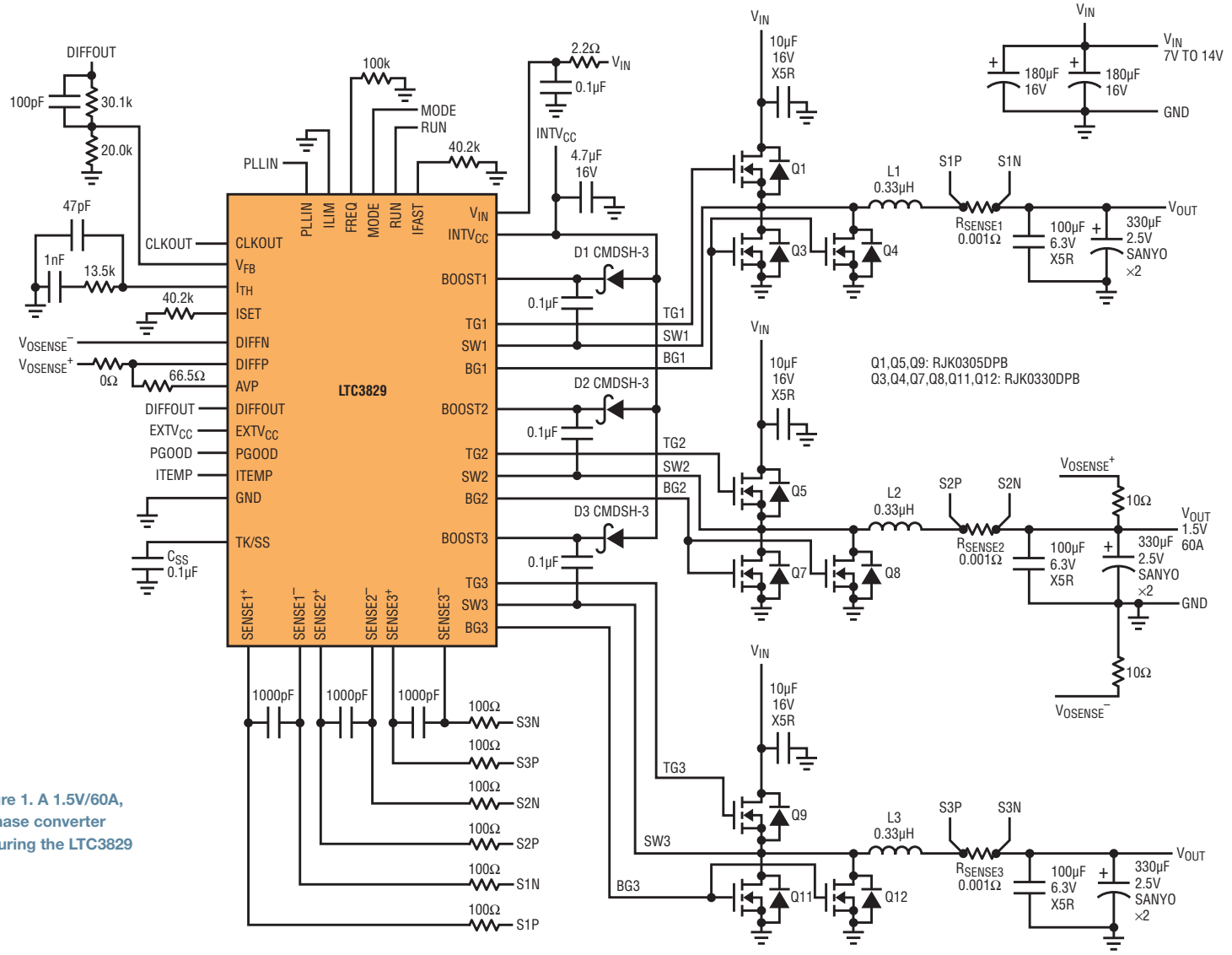


Figure 1. A 1.5V/60A, 3-phase converter featuring the LTC3829

The LTC3829's constant-frequency peak current mode control architecture allows a phase-lockable frequency of up to 770kHz. Even at this high frequency, high step-down ratios are possible, thanks to the LTC3829's ability to operate at low duty cycle due to its small minimum on-time (90ns).

LTC3829 FEATURES

The LTC3829 is a current mode PolyPhase® controller, similar to the LTC3850, but with an integrated a high speed differential amplifier for remote output voltage sensing, which can eliminate regulation errors due to PCB voltage drops at heavy loads. Figure 1 shows a typical 7V~14V input, 1.5V/60A output application schematic.

PolyPhase Operation and High Step-Down Ratios at High Frequency

The LTC3829's three channels run 120° out-of-phase, reducing input RMS current ripple, as well as the required input capacitance. The CLKOUT and PLLIN pins enable up to 6-phase operation with multiple LTC3829s.

Figure 2 shows the tightly balanced DC current sharing between stages. Dynamic current sharing is also well balanced cycle-by-cycle due to the LTC3829's peak current mode architecture.

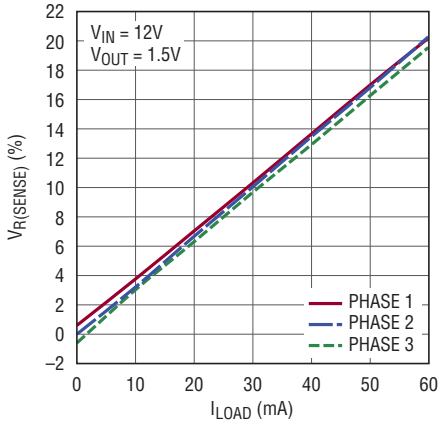


Figure 2. Current sharing performance

The LTC3829's constant-frequency peak current mode control architecture allows a phase-lockable frequency of up to 770kHz. Even at this high frequency, high step-down ratios are possible, thanks to the LTC3829's ability to operate at low duty cycle due to its small minimum on-time (90ns).

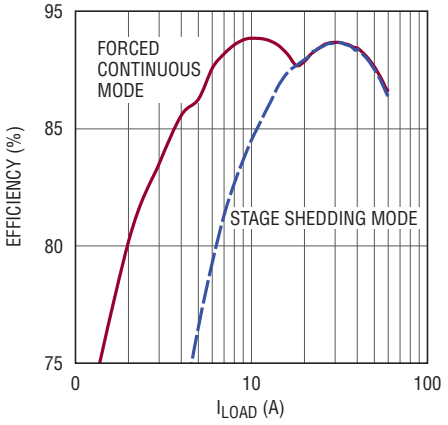
Accurate DCR Current Sensing over Temperature

The LTC3829's maximum current sense voltage is selectable—30mV, 50mV or 75mV—allowing the use of either the inductor DCR or a discrete sense resistor as the current sensing element. The inductor winding resistance (DCR) changes over temperature. So to improve accuracy, the LTC3829 can sense the inductor temperature via the ITEMP pin and maintain a constant current limit over a broad temperature range. This makes high efficiency inductor DCR sensing more reliable for high current applications.

Stage Shedding for Improved Light Load Efficiency

At heavy loads, the LTC3829 operates in constant frequency PWM mode. At light loads, it can operate in any of three modes: Burst Mode operation, forced continuous mode and Stage Shedding mode. Burst Mode operation switches in pulse trains of one to several cycles,

Figure 3. Efficiency with and without Stage Shedding mode enabled



V_{IN} = 12V
V_{OUT} = 1.5V
F_{SW} = 400kHz
L = 330nH
R_{SENSE} = 1mΩ
QT = RJK0305DPB
QB = 2xRJK0330DPB

Figure 4. Stage Shedding mode: 3-phase to 1-phase transition

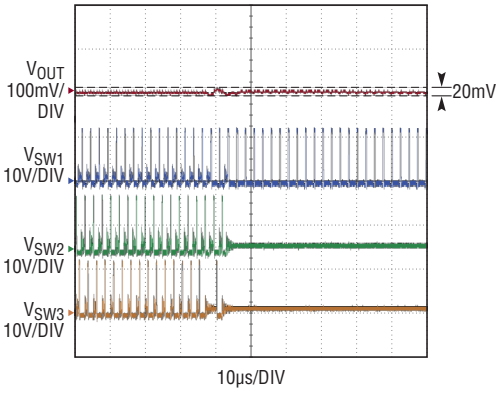
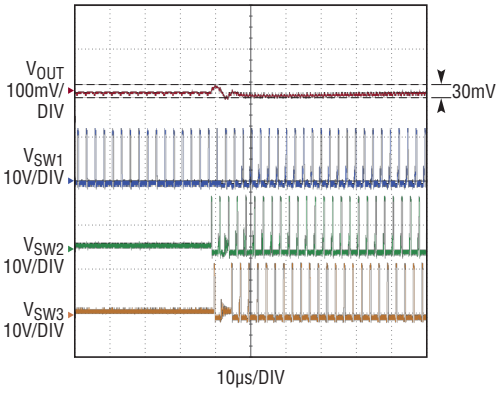


Figure 5. Stage Shedding mode: 1-phase to 3-phase transition



Linear Technology's proprietary programmable Stage Shedding feature can further improve the power supply efficiency in loads up to ~30%. At light loads, two of the three channels can be shut down in order to reduce switching-related losses.

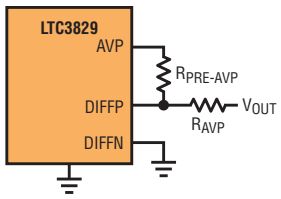


Figure 6. Programmable AVP

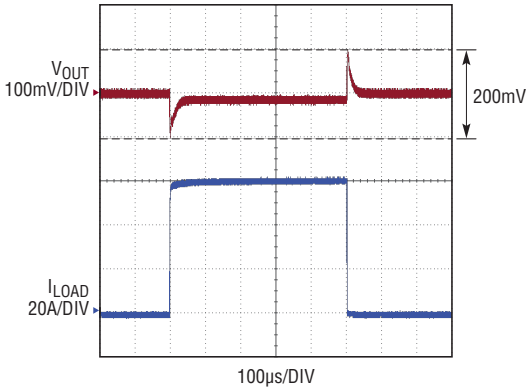


Figure 7. Transient performance without AVP

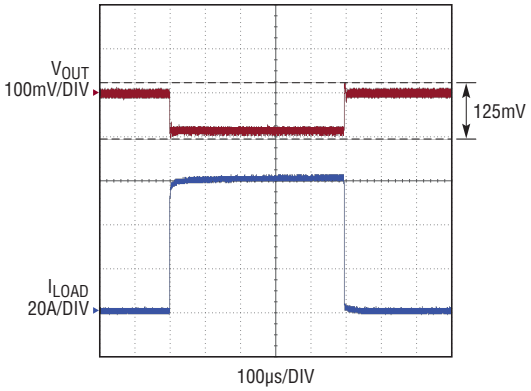


Figure 8. Transient performance with AVP

with the output capacitors supplying energy during internal sleep periods. This provides the highest possible efficiency at very light load. Forced continuous mode offers continuous PWM operation from no load to full load, providing the lowest possible output voltage ripple.

In addition, Linear Technology's proprietary programmable Stage Shedding feature can further improve the power supply efficiency in loads up to ~30% of full load as shown in Figure 3. At light loads, two of the three channels can be shut down in order to reduce switching-related losses.

When the MODE pin is tied to $INTV_{CC}$, the LTC3829 enters Stage Shedding mode. This means that the second and third channels stop switching when the I_{TH} pin voltage is below a certain programmed threshold. This threshold voltage, V_{SHED}, on the I_{TH} pin is programmed according to the following formula:

$$V_{SHED} = 0.5 + \frac{5}{3}(0.5 - V_{ISET})$$

Connecting a single resistor from the ISET pin to SGND sets V_{ISET} by way of the precision 7.5µA current source from ISET.

Stage Shedding mode in the LTC3829 features smooth transitions when dropping from 3-phase to 1-phase operation and likewise when increasing from 1-phase to 3-phases, with minimum ripple on the output, as shown in Figures 4 and 5. The smooth transition is a direct result of current mode control—a voltage mode, multiphase supply would have trouble achieving this performance.

Active Voltage Positioning (AVP)

Transient performance is a priority in high current power supply designs. To minimize the voltage deviation during load steps, the LTC3829 includes two features that lower peak-to-peak output voltage deviation for a given load step: one is the programmable active voltage positioning (AVP); the other is the programmable nonlinear control.

The AVP scheme modifies the regulated output voltage depending on its current loading. The LTC3829 senses inductor current information by monitoring voltage across the sense resistor, R_{SENSE} or the DCR sensing network of all three channels. The voltage drops are added together and applied as $V_{PRE-AVP}$ between the AVP and DIFFP pins, which are connected through resistor $R_{PRE-AVP}$. Then $V_{PRE-AVP}$ is scaled through R_{AVP} and added to the output voltage as the compensation for the load voltage drop. As shown in Figure 6, the load slope (R_{DROOP}) is:

$$R_{DROOP} = R_{SENSE} \bullet \frac{R_{AVP}}{R_{PRE-AVP}} \left(\frac{V}{A}\right)$$

With proper design, AVP can reduce the magnitude of transient induced peak-to-peak voltage spikes by 38%, as shown in Figures 7 and 8.

The LTC3829 3-phase step-down controller fits an outsized feature set into a small 5mm × 7mm 38-pin QFN, making it ideal for high current applications, including telecom and datacom systems, industrial and high performance computers.

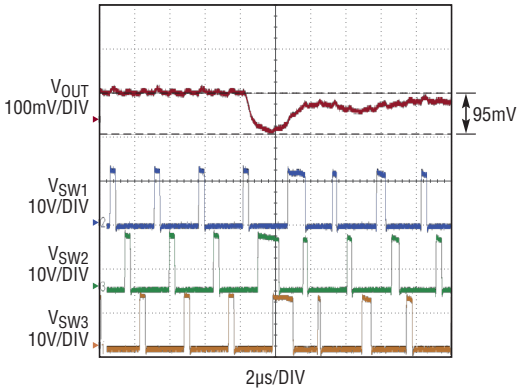


Figure 9. Transient performance without nonlinear control

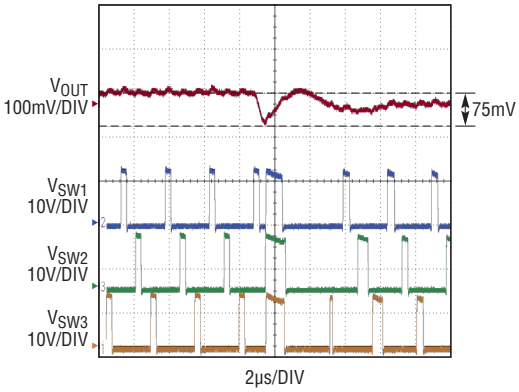


Figure 10. Transient performance with nonlinear control

Nonlinear Control

The LTC3829 features a unique nonlinear control loop that can improve transient response dramatically. In the nonlinear control loop, an internal circuit monitors the output of the error amplifier. If the amplifier is sinking or sourcing large output currents (level programmable), the supply output voltage has significant overshoot or undershoot. This is when nonlinear control takes over: the controller simultaneously turns all of the TG signals *on* at a load step up, or *off* at a load step down to avoid control loop or PWM switching cycle delays.

This feature is enabled and programmed through the IFAST pin. When the IFAST pin is tied to $INTV_{CC}$, the nonlinear control loop is disabled. The IFAST pin sources a precision 10µA, so connecting a resistor from IFAST to SGND sets V_{IFAST}. When V_{IFAST} is set below 0.5V, the difference of 0.5V and V_{IFAST} sets the threshold voltage that triggers nonlinear control. Nonlinear control is only enabled when the feedback voltage V_{FB} is within the UV and OV window.

Once nonlinear control is enabled, the top gate of all channels is turned *on* if:

$$V_{FB} = V_{REF} - \frac{0.5 - V_{IFAST}}{5} \bullet 1.2$$

The top gate of all channels is turned *off* if:

$$V_{FB} = V_{REF} + \frac{0.5 - V_{IFAST}}{5}$$

where V_{REF} is the reference voltage (0.6V).

With proper design, nonlinear control can improve transient response by 21% during the load step up transient, as shown in Figures 9 and 10.

CONCLUSION

The LTC3829 3-phase step-down controller fits an outsized feature set into a small 5mm × 7mm 38-pin QFN. It offers high efficiency with strong integrated drivers and Stage Shedding/Burst Mode operation. It supports temperature compensated DCR sensing for high reliability. Its AVP and nonlinear control can improve transient response with minimum output capacitance. Output tracking, multi-device current sharing and external sync capability fill out its menu of features. The LTC3829 is ideal for high current applications, including telecom and datacom systems, industrial and high performance computers. ■

What's New with LTspice IV?

Gabino Alonso

twitter Follow @LTspice on Twitter for up-to-date information on models, demo circuits, events and user tips: *www.twitter.com/LTspice*

LTspice® IV is a high performance SPICE simulator, schematic capture and waveform viewer specifically designed to speed up the process of power supply design. LTspice IV adds enhancements and models to SPICE, significantly reducing simulation time compared to typical SPICE simulators, allowing one to view waveforms for most switching regulators in minutes compared to hours for other SPICE simulators.

LTspice IV is available free from Linear Technology at www.linear.com/LTspice. Included in the download is a complete working version of LTspice IV, macro models for Linear Technology's power products, over 200 op amp models, as well as models for resistors, transistors and MOSFETs.

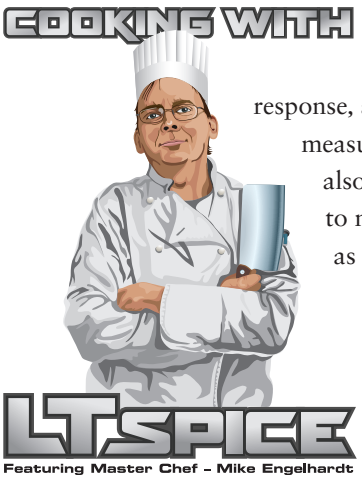
What is LTspice IV?

COOKING WITH LTspice IV SEMINAR TAKES WORLD TOUR

Mike Engelhardt, the author and creator of LTspice IV, is embarking on a world tour to teach you the ins and outs of LTspice IV in a series of free half-day seminars. At each seminar, Mr. Engelhardt will show you how to quickly simulate switch mode power supplies, compute efficiencies and observe power supply start-up behavior and transient response. You will also learn how to use LTspice IV as a general-purpose SPICE simulator for AC analysis, DC sweeps, noise analysis and circuit simulations. The presentation includes a description of the algorithms used in LTspice IV to give you a unique and powerful perspective on the inner workings of LTspice IV.

For more information on these upcoming seminars and other events please visit www.linear.com/LTspiceEvents.

Get the Schedule



NEW HOW-TO VIDEOS

One of the fastest ways to get started with LTspice IV and learn a few user tips, is to watch the instructional videos available at www.linear.com/LTspiceVideos. Two new videos are now available:

- The first new instructional video covers the *LTspice IV Schematic Editor* (video.linear.com/84). This video shows how to use the LTspice IV schematic capture program in the layout of a simple circuit so you can quickly draft and make edits to your design.
- The second video covers the *LTspice IV Waveform Viewer* (video.linear.com/88). This video shows you how to quickly probe the circuit for current and voltage response, and how to view and measure the waveforms. It also includes techniques to navigate the waveforms as you analyze results.

Two new LTspice IV how-to videos are now available

LTspice IV Schematic Editor

LTspice IV Waveform Viewer

NEW DEVICE MODELS

To update your installation of LTspice IV with the latest models, choose Sync Release from the Tools menu in LTspice IV. Here is a list of some new models:

LT3029: Dual 500mA/500mA low dropout, low noise, µpower linear regulator www.linear.com/3029

LT6109-1/LT6109-2: High side current sense amplifier with reference and comparators www.linear.com/6109

LT3970-3.3/LT3970-5: 40V, 350mA step-down regulator with 2.5µA quiescent current and integrated diodes www.linear.com/3970

LTC3618: Dual 4MHz, ±3A synchronous buck converter for DDR termination www.linear.com/3618

LT6107: High temperature, high side current sense amp in SOT-23 www.linear.com/6107

LTC4225-1/LTC4225-2: Dual ideal diode and Hot Swap controller www.linear.com/4225

LTC3867: Synchronous step-down DC/DC controller with differential remote sense and nonlinear control www.linear.com/3867

LTC3388-1/LTC3388-3: 20V high efficiency nanopower step-down regulator www.linear.com/3388

LTC3634: Dual 15V, 3A monolithic step-down regulator for DDR power www.linear.com/3634

COMPUTING THE AVERAGE OR RMS VALUE OF A TRACE IN LTSPICE IV

The LTspice IV waveform viewer can integrate a trace to produce the average or RMS value over a given region.

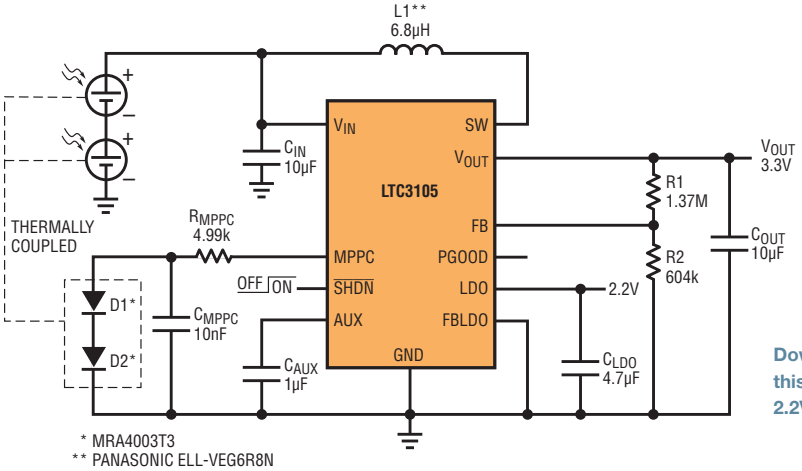
To integrate a trace in the waveform viewer:

1. Zoom in to the region of interest.
2. Hold down the control key and click the label of the trace you want to integrate.

Based on the physical units of the data trace, LTspice IV displays a meaningful average for that type of data. For example, if the units are a voltage or current, LTspice IV displays the average and the RMS values. Otherwise, LTspice IV displays the average and integral of the data displayed in the waveform viewer. If you're plotting noise densities from a .noise simulation, LTspice IV shows total RMS noise.

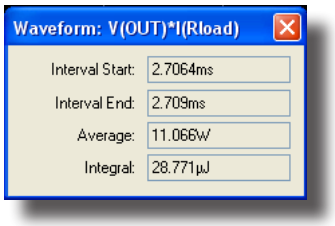
Happy simulations!

LTspice IV Power-User Tip



Download the LTspice IV demonstration circuit for this 2-cell photovoltaic to dual output, 3.3V and 2.2V, converter at www.linear.com/3105

It's easy to calculate the RMS or average value of a waveform trace in LTspice IV. For more information, see the LTspice IV Power-User Tip above.



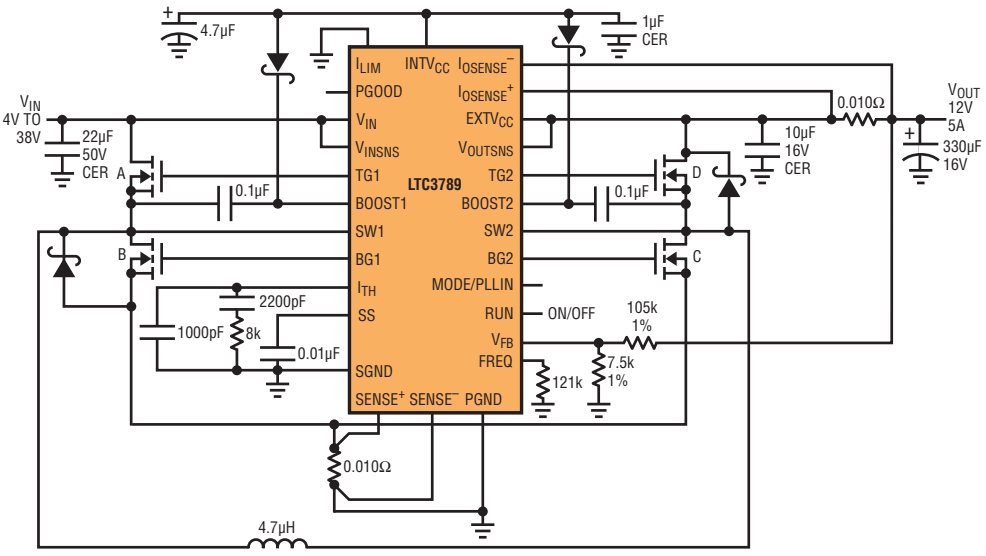
LTC3617: ±6A monolithic synchronous step-down regulator for DDR termination www.linear.com/3617

LTM®4613: EN55022B-compliant, 36V input, 15V, 8A output, DC/DC µModule regulator www.linear.com/4613

NEW LTspice IV DEMO CIRCUITS

The LTspice IV circuit collection is available at www.linear.com/DemoCircuits. Here are some of the new demonstration circuits now available:

- 36V to 12V, 8A integrated step-down DC/DC converter using the LTM4613. www.linear.com/4613
- 5V to 12V, 900mA step-up DC/DC converter using the LT3581. www.linear.com/3581
- Automotive ±30V supply protection circuit with 3.5V undervoltage and 18V overvoltage using the LTC4365. www.linear.com/4365
- 4V–15V to 1.8V, 2.5A monolithic synchronous step-down DC/DC converter using the LTC3603. www.linear.com/3603
- A 4.5V–10V to 2.5V, 2.5A monolithic synchronous step-down DC/DC using the LTC3602. www.linear.com/3602
- A dual synchronous step-up converter that takes a 5V–24V input to 24V, 3A–5A and 12V, 8A–10A using the LTC3788. www.linear.com/3788 ■



The LTspice IV demonstration circuit for this 12V, 5A automotive high efficiency buck-boost DC/DC solution with programmable output current limit is available at www.linear.com/3789

15A µModule Regulator Solves Thermal Problems by Converting 12V to 1V with High Efficiency

Eddie Beville

Advances in silicon process technology continue to reduce transistor geometries down to historical levels in microprocessors, FPGAs and ASICs. The power supply voltage levels necessary to power these large, complex digital devices also continue to shrink, creating unique power supply design challenges.

One major concern is the power regulator's conversion efficiency at low output voltages. For example a typical high efficiency switching regulator that converts 12V to 3.3V at 15A has a conversion efficiency of ~93%. For practical purposes, such a regulator incurs most of its efficiency loss due to I^2R losses. Therefore 93% efficiency for processing 49.5W to the load equates to a 3.72W loss.

Likewise, a low output voltage requirement of 1V at 15A with an efficiency of 76% incurs a power loss of 4.74W. Typical high density power solutions are challenged to achieve high efficiencies at low output voltages due to the size constraints of the power stage. The power stage must have high performance power MOSFETs and inductors to improve low voltage conversion efficiency not just an increase the solution size.

In reality, many feature-laden digital devices have current requirements in the >30A range for the low voltage supply. Thus a 76% efficiency 1V output would incur a 9.48W loss for a 30A load, which would certainly cause thermal challenges. The thermal problems multiply with the number of 30A regulators required on a system board.

Unchecked regulator power losses, when added to other system power losses create serious thermal challenges. One issue is that small-geometry ASIC or FPGA leakage currents rise with system temperature, thus compromising system performance and reliability.

One possible solution is to use a power converter module that can deliver significantly higher output power than necessary for the application, and run it at an output current point that maximizes efficiency. Of course, overly large solutions are not feasible in space-constrained systems and the current limit of this solution is much higher than the required current.

Another solution is to use a discrete power converter that is optimized for low output voltage efficiency. But again space constraints and component sourcing can be challenging. Another challenge with a discrete design is how to effectively cool it and heat sink the various discrete power components, which have different heights.

µMODULE SOLUTION

Figure 1 shows a complete 1.0V at 15A converter that uses the LTM4627 µModule regulator housed in a 15mm × 15mm × 4.32mm package. The LTM4627 integrates the high performance power path

Figure 1. A complete 1V at 15A converter requires only a few components around the LTM4627 µModule regulator, which comes in a thermally enhanced 15mm × 15mm × 4.32mm package

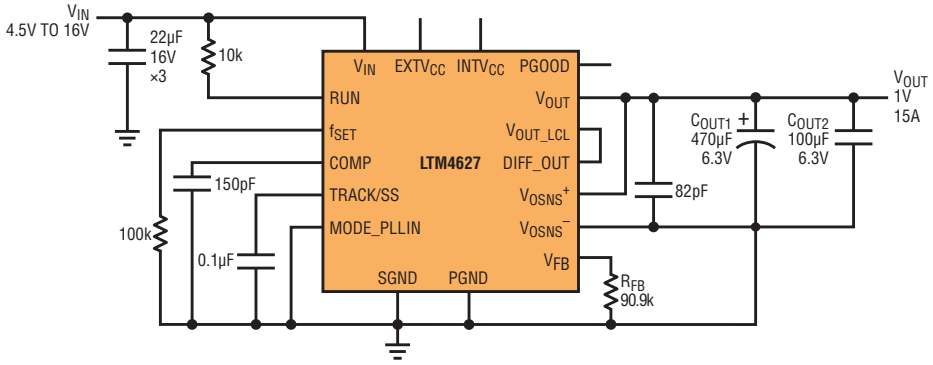
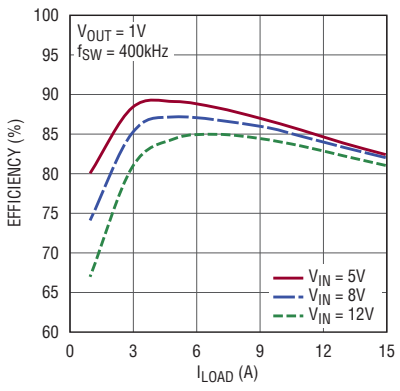


Figure 2. Efficiency of the regulator in Figure 1



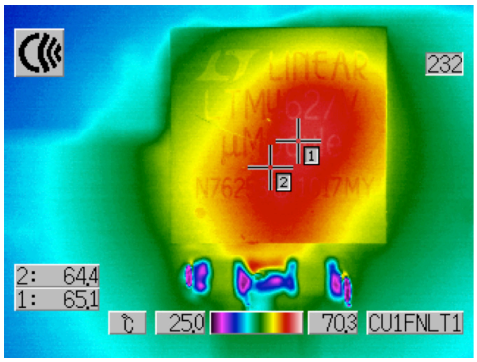


Figure 3. Thermal plot of the LTM4627 converting 12V to 1V at 15A with no forced air or heat sink

and control circuitry, thus simplifying the design to a few external bulk capacitors and a few small resistors.

The LTM4627 features include fully differential remote sensing, output voltage tracking and soft-start, high efficiency at light loads utilizing the Burst Mode operation or pulse-skipping features, voltage monitoring and frequency synchronization. The LTM4627 uses a current mode architecture, which enables multiple µModule regulators to run in parallel (Figure 5), sharing the load for increased output current with accurate current limit control.

The LTM4627 µModule regulator is optimized for high efficiency conversion to low output voltages—with a complete converter packaged in a small, thermally enhanced form factor. The input voltage range is 4.5V to 20V with output voltage programming from 0.8V to 5V. Figure 2 shows efficiencies of 82% to 83% for 1V at 15A from 5V, 8V and 12V inputs. This is an efficiency improvement of 6% to 7% over typical (and larger) solutions, or a power loss improvement of 1.68W in a small form factor.

Figure 3 shows a LTM4627 thermal plot for 12V to 1V at 15A with no airflow or heat sinking. The temperature rise is ~40°C above 25°C ambient at 65°C. The power loss of ~3W multiplied by the data sheet specified θ_{JA} thermal resistance of 13°C/W matches the 40°C rise in the thermal plot.

The LTM4627 package has a highly thermal conductive substrate with a layout that is thermally modeled and designed to enhance thermal performance and uniform heat spreading. While the package is small, it presents enough surface area to a PCB (and heat sink) to minimize the overall thermal resistance of the solution.

Figure 4 shows the LTM4627 12V to 1V derating curve. The LTM4627 can operate in higher ambient temperatures with full load capability in a very small form factor.

Figure 5 shows a 2-phase, 30A design utilizing two parallel LTM4627 µModule regulators that are clocked 180° out-of-phase using clock signals from the LTC6908-1.

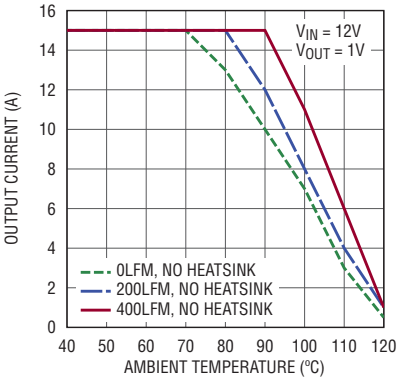


Figure 4. Derating curves for the LTM4627 converting 12V to 1V

Current sharing is well balanced during both steady state DC load and dynamic transients. The accurate remote sense amplifier yields outstanding voltage accuracy at the load point. For even higher output currents, simply add more LTM4627s.

CONCLUSION

The LTM4627 µModule regulator is a high performance versatile DC/DC converter that can be used in many applications requiring high efficiency over a wide output voltage range. The very small form factor and ease of use make the LTM4627 ideal for space-constrained designs. ■

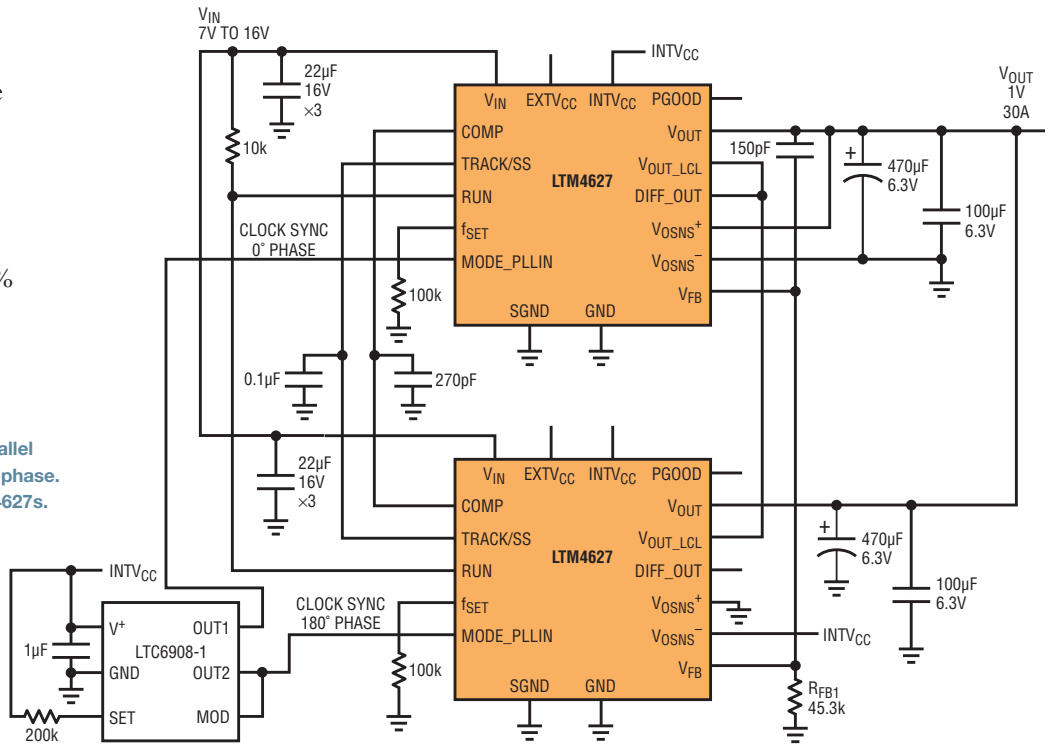


Figure 5. A 2-phase, 30A design based on two parallel LTM4627 µModule regulators clocked 180° out-of-phase. For higher output currents, simply add more LTM4627s.

Solve Isolated Control Problems by Up-Shifting Control Frequency with TimerBlox PWM Generator

Tim Regan

Industrial and medical systems often have functions that are completely isolated from the mains power—requiring control signals that must cross the isolation barrier, usually via a small transformer. One cost-effective source of control signals is the I/O pin of embedded controllers. The oscillators and counters already included in controllers can be used to produce digitally programmable PWM signals, which can provide a variable duty cycle square wave, or, if averaged by a simple RC lowpass filter, a linearly variable analog voltage.

For example, if the I/O pin output of an embedded controller produces a varying duty cycle PWM signal that switches between V_{CC} and ground, the average output voltage of the I/O pin is simply V_{CC} • (duty cycle).

The problem with using the PWM output of an embedded controller to produce control signals in an isolated system is that the frequency of these signals is often too low for a small signal transformer to handle.

Figure 1 shows a simple strategy that allows low frequency PWM signals to be properly passed via small signal

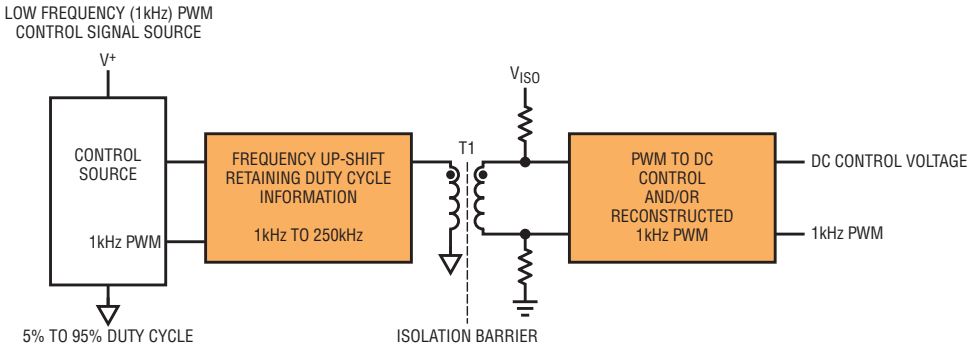


Figure 1. Transferring control information across a small signal isolation transformer requires a higher frequency PWM signal than that produced by most embedded controllers. On the isolated side, the resulting signal can be either converted to a DC control voltage or converted to a replicate of the original PWM signal.

transformers across an isolation barrier. In this solution, the low frequency PWM signal is converted to a higher frequency while retaining the duty cycle control information. Specifically, a 1kHz PWM signal is shifted to 250kHz, coupled across the isolation barrier, then shifted back down to the original 1kHz (or simply converted to a DC voltage control signal). Changes in the source PWM signal duty cycle are duplicated nearly instantly on the isolated side. Accuracy of the isolated control signal is within 1% of the source duty cycle.

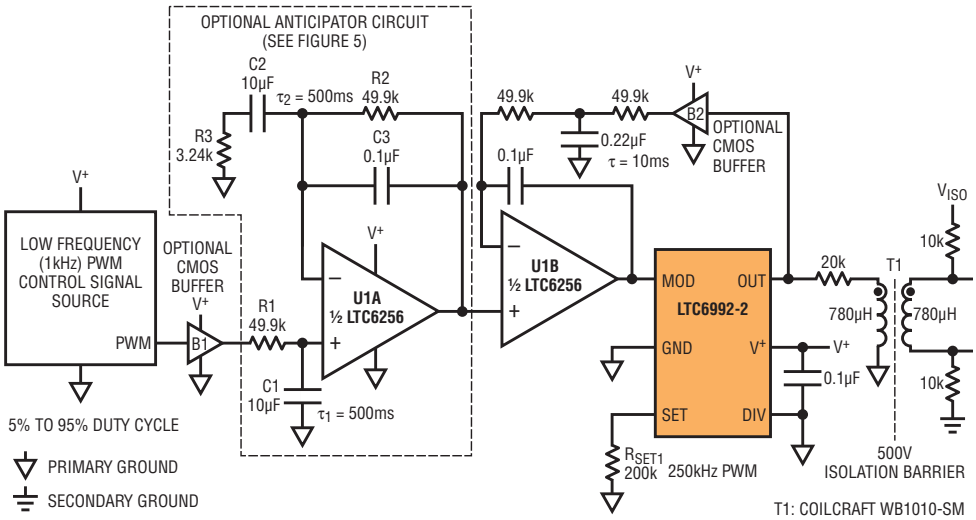


Figure 2. Nonisolated control side. A TimerBlox® PWM circuit generates a 250kHz signal with the same duty cycle as the original low frequency PWM signal. The optional anticipator circuit improves step response by anticipating step changes in the duty cycle of the control PWM (see "Circuit Enhancements" below).

The problem with using the PWM output of an embedded controller to produce control signals in an isolated system is that the frequency of these signals is often too low for a small signal transformer to handle. Here is a simple strategy that allows low frequency PWM signals to be properly passed via small signal transformers across an isolation barrier.

UP-SHIFTING THE PWM CONTROL FREQUENCY

Figure 2 shows a circuit that converts a 1kHz PWM signal to a 250kHz signal with the exact same duty cycle. This 250kHz signal can easily couple across an isolation transformer.

The LTC6992-2 is a voltage-controlled PWM generator. A voltage ranging from 0V to 1V on the MOD input pin linearly varies the duty cycle of the output clock from 5% to 95%. This device is chosen because it keeps its output clocking at all times. The duty cycle never reaches 0% or 100% duty cycle, since a DC signal would not pass through the transformer. The output frequency can range up to 1MHz and is easily programmed using resistors. Resistor R_{SET} fixes an internal master oscillator frequency and the voltage on the DIV pin sets an internal frequency divider ratio.

Amplifier U1B (one half of an LTC6256 low power dual rail-to-rail op amp) is an integrator used to servo the voltage at the MOD pin to force the 250kHz signal duty cycle to match the 1kHz input signal duty cycle. Simple RC lowpass filters convert both PWM clocks to their average DC voltages. To minimize duty cycle jitter, the time constants of these filters should be much longer than the clock period. The 1kHz PWM signal is filtered with a 500ms time constant network while the 250kHz filter is 10ms. The integrator output voltage stops at the MOD pin voltage required to force the average voltages, and therefore the duty cycles, of the two PWM signals to be exactly the same.

For accurate duty cycle control, the amplitudes of the two square waves must be the same so the power supply voltage for the LTC6992-2 is the same supply used for the controller generating the input PWM signal. The LTC6992-2 has 20mA of output current drive and can directly drive the primary winding of the isolation transformer.

The 500ms time constant network on the control source PWM signal makes duty cycle changes occur at a slow rate. Amplifier U1A is an optional circuit function that can speed up the response time of the circuit to duty cycle changes by a factor of 10. This function is described in the section "Circuit Enhancements," below.

CONTROL SIGNALS ON THE ISOLATED SIDE

On the isolated side of the transformer is an LT1719 comparator. This comparator converts the signal across the secondary of the transformer to a 250kHz square wave. This square wave can be filtered and simply buffered with an op amp to provide an isolated DC control voltage that moves proportionally to the duty cycle of the original PWM signal.

If a reconstructed replica of the 1kHz input PWM signal is required on the isolated side, simply add another LTC6992-2 PWM circuit, which is resistor programmed to output a 1kHz PWM signal. An integrator can be used here, in the same fashion as on the nonisolated side, to servo the output duty cycle to match that of

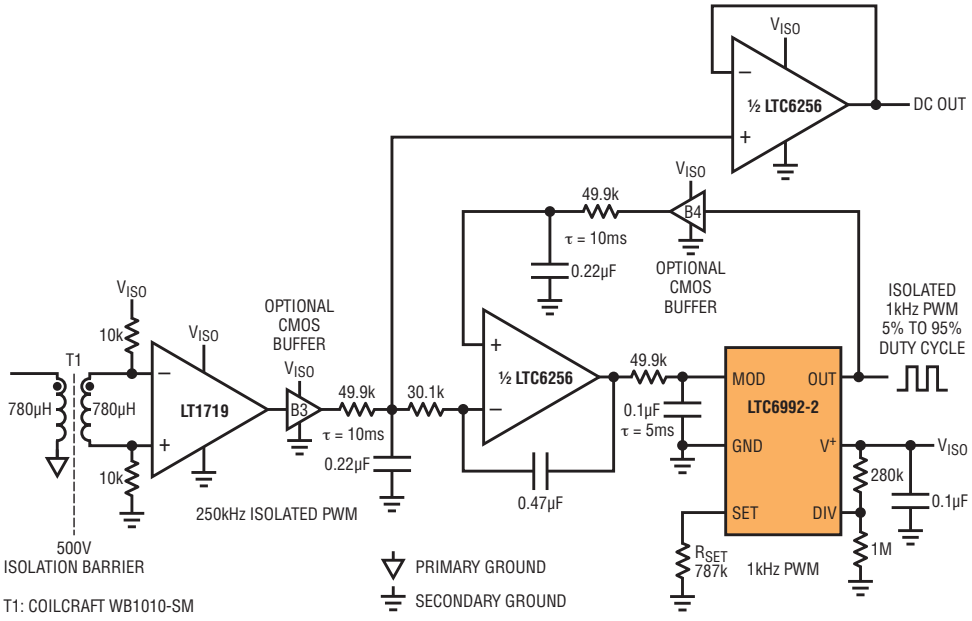


Figure 3. Isolated side. Simply buffering the filtered average of the 250kHz PWM signal on the isolated side provides a DC control signal. A second TimerBlox circuit can be used to reconstruct the original 1kHz PWM signal with the same duty cycle as the control source signal.

A possible drawback to this circuit is the long time constant and resulting slow response time to any changes in the duty cycle of the 1kHz control source PWM signal. The amplifier circuit shown in Figure 5 allows the 250kHz PWM signal to respond nearly instantly to any changes in the 1kHz control PWM despite the slow filter response time.

the 250kHz comparator output square wave. Once again the average voltages, and therefore the duty cycles, of the two square waves are forced to be the same.

CIRCUIT ENHANCEMENTS

Improving Duty Cycle Accuracy

One important requirement for an accurate match of the two duty cycles is that the amplitude of the PWM signals are exactly the same. Lightly loaded CMOS outputs swing virtually all the way between ground and the supply rail.

For more precise matching of the amplitudes of the two PWM signals, some inexpensive CMOS logic buffers, B1 and B2 in Figure 2 and B3 and B4 in Figure 3 on the isolated side, can be used on each square wave signal to force the amplitudes to be identical. Two like buffers powered from the same supply with the same current loading will produce matched output levels. Any supply voltage variation moves each of the two compared signals the same amount for a good measure of supply variation insensitivity.

Figure 4 shows the duty cycle difference between the source-side PWM and the replicate isolated-side PWM—results are shown with and without the amplitude-matching logic buffers.

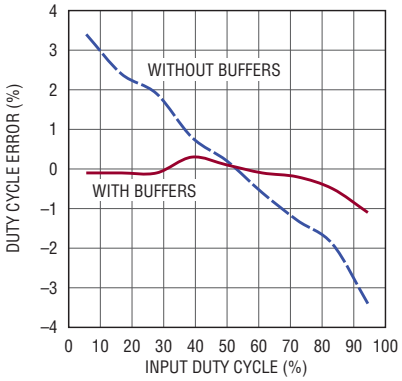


Figure 4. Using simple CMOS buffers to match the amplitudes of all PWM signals can reduce duty cycle error to less than 1%.

Anticipator Amplifier Predicts and Speeds Response to the Final Value

A possible drawback to this circuit is the long time constant and resulting slow response time to any changes in the duty cycle of the 1kHz control source PWM signal. The amplifier circuit shown in Figure 5 allows the 250kHz PWM signal to respond nearly instantly to any changes in the 1kHz control PWM despite the slow filter response time.

Circuit operation relies on knowing the exact time constant of the exponentially responding input signal, τ_1, which is set at 500ms by R1 and C1. Any step change in duty cycle of the PWM input signal creates a voltage at the plus input of the amplifier that changes from an initial voltage, V_i, to a final voltage, V_f, in an exponential fashion per the familiar equation:

$$V_{IN} = V_f - (V_f - V_i) \bullet e^{-t/\tau_1}$$

The time domain step response at the output of this circuit can be found by the following series of equations:

$$V_{OUT} = V_{IN} + R2 \bullet I_{C2}(t)$$

$$I_{C2}(t) = C2 \bullet \frac{dV_{IN}}{dt}$$

Recall from the math that:

$$\frac{dae^x}{dt} = ae^x \bullet \frac{dx}{dt}$$

so

$$\frac{dV_{IN}}{dt} = -(V_f - V_i) \bullet e^{-t/\tau_1} \bullet \frac{-1}{\tau_1}$$

$$= \frac{1}{\tau_1}(V_f - V_i) \bullet e^{-t/\tau_1}$$

continued on page 43

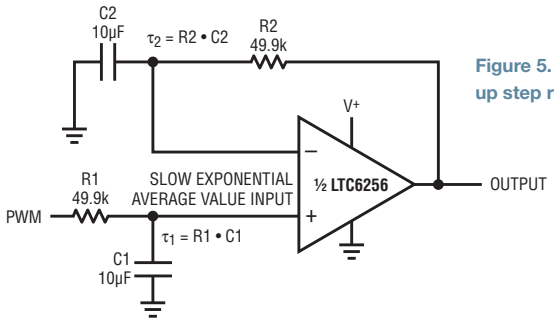


Figure 5. Anticipator amplifier circuit speeds up step response by a factor of 10.

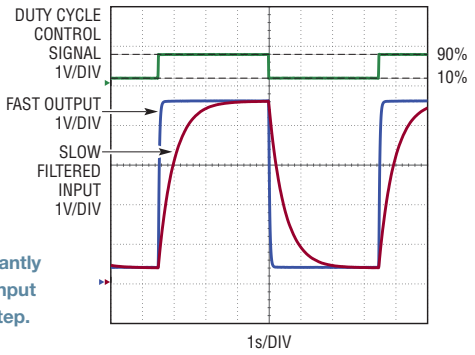


Figure 6. The anticipator output moves nearly instantly to the final value of a slow changing exponential input signal. Input change is a 10% to 90% duty cycle step.

Product Briefs

OP AMP DRIVES SAR ADCs TO TRUE ZERO ON A SINGLE 5V SUPPLY

The LTC6360 is a very low noise, high speed amplifier that can drive to 0V while maintaining high linearity on a single 5V supply. The LTC6360's integrated ultralow noise charge pump provides an internal negative rail, eliminating the need for a negative supply. Compared to typical rail-to-rail output single-supply amplifiers that can only swing to within a few hundred millivolts of ground, the LTC6360 provides improved linearity and dynamic range in applications that benefit from a true zero output swing.

The LTC6360 achieves outstanding precision and is ideal for driving 16- and 18-bit SAR ADCs (successive approximation register analog-to-digital converters). Input offset voltage is less than 250µV max, and noise is only 2.3nV/√Hz, providing excellent dynamic range. The device settles to 16-bits in 150ns, and achieves a closed loop –3dB bandwidth of 250MHz. Harmonic distortion (HD2/HD3) is –103dBc/–109dBc at f_{IN} = 40kHz. The LTC6360 is unity gain stable, allowing it to be used as a buffer to achieve the lowest output noise. The output is designed to drive a series 10Ω resistor and 330pF capacitor filter network, although larger load capacitances can be driven.

The LTC6360 is available in a compact 3mm × 3mm, 8-pin leadless DFN package and an 8-pin MSOP package with exposed pad and operates over a –40°C to 125°C temperature range.

ULTRALOW NOISE AND SPURIOUS 0.37GHZ TO 5.7GHZ INTEGER-N SYNTHESIZER WITH INTEGRATED VCO

The LTC6946 is a high performance, low noise, 5.7GHz phase-locked loop (PLL) with a fully integrated VCO, including a reference divider, phase-frequency detector (PFD) with phase-lock indicator, ultralow noise charge pump, integer feedback divider, and VCO output divider. The charge pump contains selectable high and low voltage clamps useful for VCO monitoring. The integrated low noise VCO uses no external components. It is internally calibrated to the correct output frequency with no external system support. The part features a buffered, programmable VCO output divider with a range of 1 through 6, providing a wide frequency range. ■

(TimerBlox, continued from page 42)

$$I_{C2}(t) = C2 \bullet \frac{dV_{IN}}{dt} = \frac{1}{\tau_1}(V_f - V_i) \bullet e^{-t/\tau_1}$$

$$V_{OUT} = V_f - (V_f - V_i) \bullet e^{-t/\tau_1} + R2 \bullet C2 \bullet \frac{1}{\tau_1}(V_f - V_i) \bullet e^{-t/\tau_1}$$

If τ_2 (R2C2) is exactly equal to τ_1 (R1C1) then:

$$V_{OUT} = V_f - (V_f - V_i) \bullet e^{-t/\tau_1} + (V_f - V_i) \bullet e^{-t/\tau_1}$$

$$V_{OUT} = V_f$$

When the input starts to change at an exponential rate, the circuit extrapolates the final value and jumps there instantly. This look-ahead response drives the duty cycle servo integrator in Figure 2 to quickly change the 250kHz PWM generator to its final value without waiting for the 500ms time constant filter to get there.

The closed loop gain of this stage increases directly with frequency and is inherently unstable. Frequency response shaping is accomplished in Figure 2 via R3 and C3. The low frequency step response is still dominated by R2 and C2.

Figure 6 shows the quick response to a step change in control signal duty cycle from 10% to 90%. The anticipated output arrives at the final voltage in about 200ms, ten times faster than the two to three seconds for the input signal to fully settle.

CONCLUSION

Generating control signals across an isolation barrier from a low frequency PWM control source can be implemented by up-shifting the PWM frequency. The LTC6992-2 PWM TimerBlox function easily handles frequency scaling with simple resistor programmability. Op amp integrators ensure that the duty cycle control information is accurately reproduced on the isolated side. ■

MOTOR PROTECTION/REGULATION

The LTC2991 is used to monitor system temperatures, voltages and currents. Through the I²C serial interface, the eight monitors can individually measure supply voltages and can be paired for differential measurements of current sense resistors or temperature sensing transistors. Additional measurements include internal temperature and internal V_{CC}.

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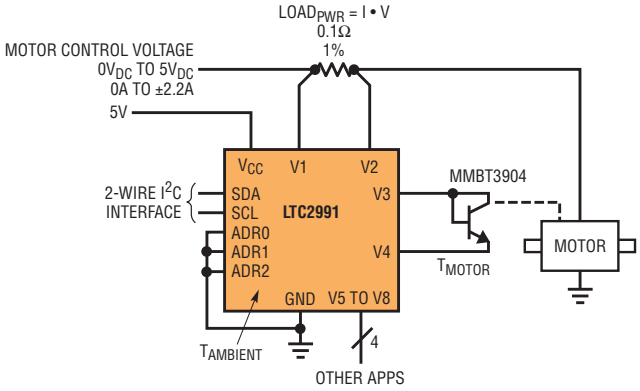

VOLTAGE, CURRENT AND TEMPERATURE CONFIGURATION:
CONTROL REGISTER: 0x06: 0xA1

$T_{AMBIENT}$	REG 1A, 1B:	0.0625°C/LSB
V_{MOTOR}	REG 0A, 0B:	305.18µV/LSB
I_{MOTOR}	REG 0C, 0D:	194.18µA/LSB
T_{MOTOR}	REG 1A, 1B:	0.0625°C/LSB
V_{CC}	REG 1C, 1D:	2.5V + 305.18µV/LSB

CIRCUIT FAULT PROTECTION WITH VERY FAST LATCHING LOAD DISCONNECT

The LT6108 is a complete high side current sense device that incorporates a precision current sense amplifier, an integrated voltage reference and a comparator. Two versions of the LT6108 are available. The LT6108-1 has a latching comparator and the LT6108-2 has a non-latching comparator. In addition, the current sense amplifier and comparator trip point are configured by external resistors.

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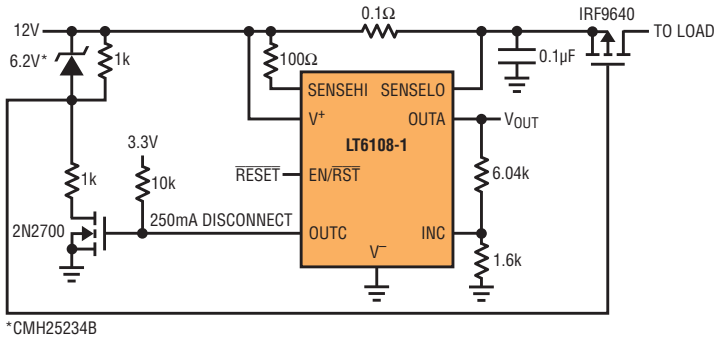

LI-ION BACKUP SUPPLY

The LTC3226 is a 2-cell series supercapacitor charger with a backup PowerPath controller. It includes a charge pump supercapacitor charger with programmable output voltage, a low dropout regulator, and a power-fail comparator for switching between normal and backup modes. The constant input current supercapacitor charger is designed to charge two supercapacitors in series to a resistor-programmable output voltage from a 2.5V to 5.3V input supply. The charger input current limit is programmable by an external resistor at up to 315mA.

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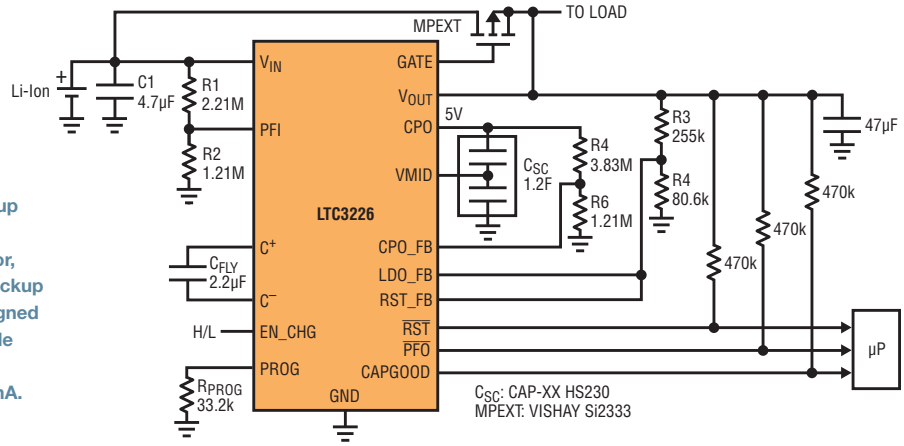

Linear Technology Corporation
1630 McCarthy Boulevard, Milpitas, CA 95035
(408) 432-1900
www.linear.com